DESIGN, SYNTHESIS, AND OPTIMIZATION OF SINGLE-/TWO-STAGE CMOS OP-AMPS

by

Pawan Kumar Dwivedi

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KANPUR

JANUARY, 1999

DESIGN, SYNTHESIS, AND OPTIMIZATION OF SINGLE-/TWO-STAGE CMOS OP-AMPS

A Thesis submitted

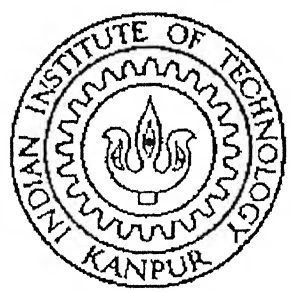
in Partial Fulfillment of the Requirements

for the degree of

Master of Technology

by

Pawan Kumar Dwivedi



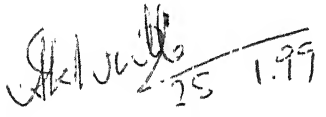
to the

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY, KANPUR

January 1999

Certificate

This is to certify that the work contained in the thesis entitled **"Design, Synthesis, and Optimization of Single-/Two-stage CMOS Op-Amps"** by **Pawan Kumar Dwivedi** has been carried out under my supervision and that this work has not been submitted elsewhere for the award of a degree.



(Dr. Aloke K. Dutta)
Associate Professor
Department of Electrical Engineering,
Indian Institute of Technology, Kanpur

January 1999.

Acknowledgements

I take this opportunity to express my deepest gratitude to Dr. Aloke K. Dutta for permitting me to do the M.Tech. Thesis under his supervision. His invaluable words have always inspired me to work properly and consistently. It has been a very nice experience for me to work under his guidance.

I express my sincere regards to my teachers Dr. M. B. Patil, Dr. S. Kar and Dr. Subir Roy whose courses have raised my knowledge-level.

There is a long list of those who helped me at different stages of the thesis. It will occupy more space if I mention their names. Finally, a special thanks to my friends Ravi, Jay, Pratul and Ritesh who made my stay at IIT Kanpur, a pleasurable and enjoyable one.

Pawan Kumar Dwivedi

Abstract

As a consequence of the emergence of a number of mixed-signal applications such as in telecommunication, signal processing, voice recognition, artificial vision, computer interfaces etc., more and more thrust is being put currently on the analog design. It is because of the kind of complexity involved in analog design, the need for automating several parts of the analog design in the overall design, comprising of both analog and digital parts onto a single chip, is being felt. At the start of the 1990's, a number of analog synthesis tools came into existence, which are mainly knowledge-based, however, they failed to deliver the required objectives. In our work, we have considered a very basic analog building block, i.e., the op-amp, which is an indispensable ingredient in most of the complex analog blocks. Their design and synthesis procedures under various specifications and constraints, such as minimum power and area, high bandwidth, high gain and high unity gain frequency, and high slew rate have been considered in this work. These design methodologies and synthesis algorithms may be extended to other analog blocks as well, with proper modifications. For each design of the op-amp considered in this work, synthesis starts with a set of input specifications. An optimization routine developed in this work equip the user with the probable values of the design variables (e.g.,

channel lengths and widths of individual transistors, bias currents, compensating capacitor values, etc.), which would satisfy the constraints. These design variables are then fed to a SPICE file for the verification of the design. The results obtained from the designs showed an excellent match when compared with the SPICE results for each such design.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The fact that the human designer operates comfortably with ensembles of active elements in an electronic circuit in the range of six to ten elements or less necessitates the automation for very complex systems having millions of components. When the idea of electronic integration came into reality, it was thought unanimously that all electronics could be implemented using digital circuitry alone. Therefore, much more attention was devoted to digital design automation and comparatively little attention was paid to its analog counterpart. Owing to the fact that the world is inherently analog in nature (I-V characteristics of semiconductor devices, speech signal as a function of time, etc. are the best citable examples of analog/continuous nature of the world), an ever increasing number of ASIC (Application Specific Integrated Circuits) designs would invariably incorporate some amount of analog circuitry in them. Also, with the opening up of a number of mixed-signal applications such as in telecommunication, signal processing, voice recognition, artificial vision, computer interfaces, etc., the Universities and the industries

are putting more and more thrust on analog design automation.

Further, recent advancements in the VLSI technology allow the merger of whole mixed-signal systems comprising of both digital and analog parts onto a single chip (known as the System on a Chip (SOC)) - a demand made by customers calling for greater speed and density on one hand, with reduced power, lower chip counts and less cost on the other. Also, it has become very obvious that although the analog part on such a chip would occupy very little area (typically of the order of 10% of the total area) as compared to the digital part, it is the design of the analog part of such a chip which is much more time consuming (typically of the order of 75-90% of the total design time) and error-prone in the overall design process. In order to meet the growing demand of analog design automation, several attempts have been made to speed up the process by automating the analog design, such as breaking the complete block into separate modules, the design of such individual modules, and the automatic layout of the often used modules.

The first analog compiler came into existence in the mid-1980's. At the start of the 1990's, a number of analog synthesis tools came into existence. These systems are mainly knowledge-based. In fact, the reason for this lies in the fact that the analog circuit design by itself is the most knowledge intensive task. These systems require the knowledge, created by a good analog circuit designer, in terms of the analytical equations describing the behaviour of the analog system completely. These systems are not able to automatically generate the appropriate analytical equations for the various analog systems. Given a circuit specification from an IC designer, they provide the corresponding dimensioned circuit descriptions (e.g., the individual transistor aspect ratios, i.e., their width (W) and length (L), bias currents,

compensating capacitor values, etc.).

These systems include the IDAC (Interactive Design for Analog Circuits) system [1] from CSEM (Centre Suisse d'Electronique et de Microtechnique S. A.), the OASYS (Operational-Amplifier Synthesis System) [2] from Carnegei-Mellon University, the OPASYN system [3] from University of Berkeley, the ARIADNE system [4] from University of Lueven, and the TOPICS system [5] from University of Eindhoven [1]. All these systems apply analog knowledge expressed in terms of analytical expressions, heuristic rules, or predefined topologies, and lead in a number of steps to appropriate dimensioned circuits. It is noteworthy that only a few of these have made successful inroads into the market, the majority being the products of the Universities, suggesting that certain important issues have still remained unresolved.

The IDAC system [1] utilises the systematic approach. It consists of a library of well engineered analog circuits, and makes use of three types of knowledge, i.e., knowledge specific to the schematic, general circuit knowledge (for example, how to size cascode devices), and knowledge common to a family of circuits (for example, how to stabilize an op-amp, how to improve the slew rate, etc.). It is not fully based on strict hierarchical decomposition, especially for modules such as op-amps, comparators, etc. It is based on the belief that there are too many electrical interactions between the various subparts of these modules to split them up hierarchically. For larger modules, however, it does apply selection/translation principles in order to keep the knowledge well organised.

[1] There is a long list of other available analog synthesis tools, such as MIDAS [6] (for op-amps), ADORE [7] (for switched capacitors), CADICS [8] (for A/D converters), etc. However, very little operational details of these tools are available in literature.

The OASYS [2] supports a high level circuit synthesis for specific classes of circuits. The methodology used in it is to describe the knowledge in a strict hierarchical fashion. From an input set of performance specifications, the appropriate topologies and the dimensions of all the components, via selection and translation steps[2], are derived (the same approach is also followed by MIDAS [6]). For an input consisting of detailed performance specifications, it produces a sized-transistor level circuit schematic. The approximate models for the given behaviour are used in order to simplify the analytical formulation of the behaviour. The framework has many similarities to some knowledge-based design ideas. The addition of a new topology requires an explicit representation of the knowledge about the circuit behaviour, heuristic design decisions, and performance trade-offs. This complicates the inclusion of new circuit topologies to the OASYS system. Besides, no optimization is performed on any level in the hierarchy. Only some limited iterations are included in the design phase.

The OPASYN [3], an automatic synthesis tool for op-amps, consists of an internal database and three functional modules: a circuit selection module, a parametric circuit optimization module, and a layout generation module. The database contains the necessary design knowledge for each op-amp topology available to the users of the system. Synthesis starts from a set of op-amp performance specifications. Based on the general domain of the specifications, the programme selects an appropriate option out of the database of generic, widely applicable op-amp topologies, unless the user explicitly specifies a particular circuit topology to be used. For the chosen circuit, optimal

[2]The process of transfer of the performance specifications for a high-level block into the performance specifications for its each subblock is termed as the translation step. The output of a translation task is a set of designed subblocks, specifically, a set of input specifications for each subblocks. The process then may be repeated inside each subblock.

values for its design parameters are determined in order to meet the objectives implied by the given specifications. Like IDAC, it is also not fully based on strict hierarchical decomposition.

The ARIADNE [4] is an analog design system for analog functional modules such as op-amps, comparators, buffers, filters, data converters, etc. The use of declarative models together with symbolic simulation provides an easy interface for the designer to include new design knowledge and circuit schematics himself, making ARIADNE an open and extendable system The system generates the topology, for which the optimal values of the individual transistor aspect ratios are obtained, which, in turn, are used for the layout generation. The key behind the synthesis is to clearly separate the knowledge (both analytic and heuristic) about the analog behaviour from the procedures that actually carry out the synthesis. The knowledge about the circuit is generally described by equations, which are grouped in the so-called declarative equation-based models (DEBMs).

For automation, circuit synthesis provides for a better solution than circuit analysis. Circuit analysis applies well known circuit principles in order to estimate the electrical behaviour, and many of these begin after partitioning larger circuit into ensembles of active elements in the range of six to ten or less. Circuit synthesis, an important approach to design, on the other hand, takes electrical behaviour as the input and by proper arrangement of circuit primitives with known properties in a suitable structure meets the desired electrical behaviour. The synthesis paradigm involves analysis but in reality, it is much more than that in the sense that it may require considerable nonlinear analysis, precise technological modelling, or an unusual circuit topology. To put it more succinctly, synthesis requires the skills in three areas:

judgment in assessing specifications, knowledge of circuit topologies, and of course, knowledge in circuit analysis.

Analog design is perceived to be one of the most knowledge-intensive design task, requiring highly skilled designers who are most accustomed to exercising their creativity on a sheet of paper. Most of the methods to synthesize analog circuits rely on having some underlying methods in order to predict the performance of a circuit as a function of the various design variables; e.g , the device sizes, the bias currents, the compensating capacitor values, etc. Thus, the two distinguishing characteristics of most analog synthesis systems are how performance is predicted and how the values of the design variables are determined. For example, one approach to performance prediction is to use a circuit simulator. Unfortunately, due to the large computational cost of circuit simulation, only a limited number of design variables can be explored in the design space. Therefore, unless it is provided with a good initial guess for the design variables (for op-amps, these are aspect ratios, bias currents, etc.), the design optimizer may fail to converge to a good solution, even when one exists.

Present analog design practice is solely based on a traditional approach of a highly heuristic nature, and therefore, bears no fruit as a basis of design automation. The approach lacks reproducibility in making various design steps explicit, particularly so while designing under several conflicting constraints. Trends in design of the analog circuits so far show that its most remarkable common feature has been a paradigmatic approach rather than systematically using general methods in order to solve electronic design problems, then intuitively or routinely selecting circuit topologies and analysing their behaviour with respect to the bigger domain. In other words, in order

to design a complex system, low-level circuits are built, tested, verified, and assembled hierarchically from the bottom-up until the first level decomposition blocks are reached. Such an approach lacks practical relevance. For example, active filter design emphasizes the network-theoretical aspects more than the information-processing aspects. Since electronic circuits are widely used to process the information, it is mandatory to take the information to be processed as the starting point for a design approach. This explains the relatively poor acceptance of the present analog circuit synthesis tools which are in a quite primitive state in comparison to the digital synthesis tools. Structured abstraction and hierarchy, a commonplace in digital domain, are absent in today's analog domain.

At present, analog cell libraries are also not as rich as the digital ones, which also gives an indication towards the present state of analog design automation. The analog circuit designers are allowed to have only crude trade-offs (design of op-amp involves many trade-offs, e.g., amplifier bandwidth versus bias current, slew rate versus bias current, and amplifier bandwidth versus transistor cut-off frequency, etc.) while designing blocks under certain performance specifications (for op-amp, these are dc gain, gain-bandwidth, slew rate, common mode rejection ratio, etc.), and these cell libraries become obsolete more rapidly in the face of technological evolution as compared to the digital libraries.

It is noticeable that full automation is proving to be unachievable for all analog circuits, owing to the fact that the amount of creativity and complexity needed to master the design of analog circuits is extremely high. It is also important to note that there is no widely accepted analog synthesis tool as of now, and research work is currently being pursued at various Uni-

versities in order to come up with a cost effective and reliable tool. In order to meet the demand of the industry and also to start the research in this area at IIT Kanpur, our effort is to carry out synthesis and optimization of certain very basic analog circuits which find enormous applications in mixed-signal systems. The very first attempt was made by Vishal and Rajeev in their B. Tech. Project entitled "Approaches to Design Automation - a case study" [9] at I.I.T. Kanpur.

The behavioural models for the apparently simple analog functions must not only include the first-order behaviour, but also the second-order effects in order to have a realistic prediction of performance of the overall system. To come up with a viable solution, the general strategy is to:

- find the best mathematical representation describing the behaviour of the circuit, and develop a realistic model of the circuit,

and

- use the chosen mathematical expressions to obtain a set of design parameters which will make the whole system meet its performance specifications.

The most widely used analog building block is the op-amp, which is almost an indispensable ingredient of all analog systems, in particular, A/D and D/A converters and filters. This makes the efficient and optimal design of op-amps very crucial and challenging. Realising the immense importance of op-amps in analog systems, we have decided to go ahead with the design and synthesis of this very basic analog building block. Synthesis of op-amps shows the nature of intricacies involved in the design of analog circuits; parameters of the op-amp track in different directions and optimization proves to be a challenge. More detailed explanations about the design and synthesis

procedures of an op-amp are given in the subsequent chapters. In particular, we have considered the synthesis procedure for op-amps under the constraints of minimum power and area, high bandwidth, high gain and bandwidth, and high slew rate specifications.

Chapter 2 explains the design aspects of CMOS op-amps for minimum power and area. A model for the channel length modulation parameter λ and the synthesis procedure for the simple current mirror have also been developed in this chapter. Chapter 3 deals with the design aspects of CMOS op-amps for high bandwidth (or unity gain frequency), where a more realistic approach has been adopted by incorporating the effect of the individual transistor's aspect ratios on the overall bandwidth of the op-amp. Chapter 4 gives the detailed design aspects of CMOS op-amps for high gain and bandwidth. Chapter 5 deals with the design aspects of CMOS op-amps for high slew rate. The results and discussion for each such design and synthesis are provided in the respective chapters. Summary and conclusion are given in Chapter 6.

Figure 1.1 depicts the block diagram for the design methodology and the synthesis algorithm adopted in this work. Our strategy to synthesize the op-amp starts with the input electrical specifications, e.g., dc gain, gain-bandwidth product, slew rate, etc. Depending upon the requirements and the constraints, the behaviour of the op-amp is represented in terms of mathematical expressions. Also, technological parameters (for example, the device transconductance parameter, the threshold voltage, the channel length modulation parameter, the device capacitances, etc.) are fed to the optimization routine from a technology file, making the whole design slightly technology independent[3]. Afterwards, a programme written in the C-language performs

[3]This makes it possible to use the same optimization routine for different technologies

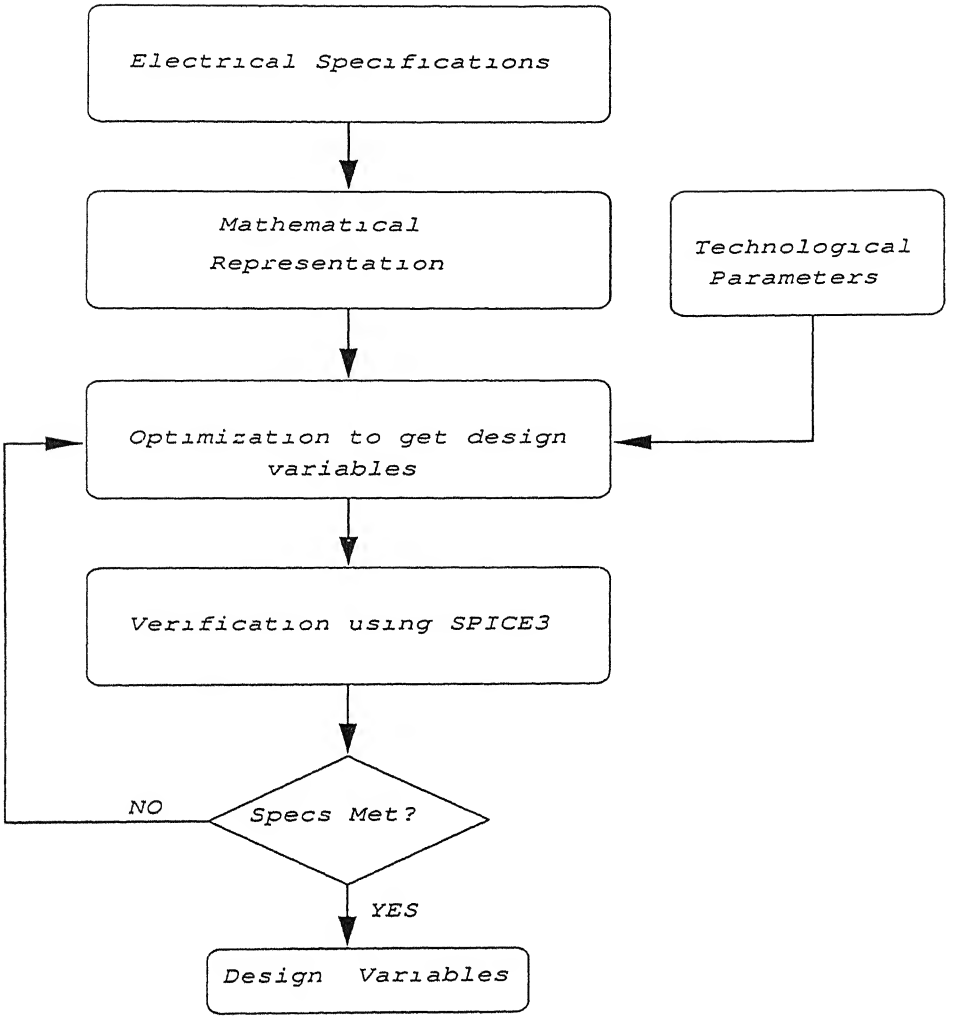


Figure 1.1: Block diagram for the design methodology and the synthesis algorithm adopted in this work.

the optimization, and the design variables obtained from the programme are fed to a SPICE file in order to do the verification of the synthesis performed. In other words, the synthesis in this work is performed in the following three phases:

- mathematical conceptualization of the op-amp, depending on the electri-

like 3 μm, 1 μm, 0.5 μm, etc., by suitably changing the technology file.

cal specifications,

- optimization under the purview of the requirements and the constraints, and
- cross-verification of the synthesis using SPICE3 [10].

Our approach is not exactly automation, rather it is a stepping stone towards that. In other words, our attempt is to provide reliable and useful synthesis procedures for op-amps, designed for minimum power and area, high bandwidth, high gain and bandwidth, and high slew rate. In this work, we have made an attempt to look at the synthesis problem in a more systematic way rather than in a heuristic way. This approach requires a good knowledge of analog circuit design, as well as skilled programming. The synthesis procedure developed/discussed in this work should be seen as initial examples aimed towards the development of an extensive synthesis procedure for op-amps. The results of our synthesis procedures for op-amps have turned out to be quite satisfactory, since the percent error between the results obtained from our design and the SPICE simulation is less than 6% for all the designs of the op-amps in this work. The possible changes/improvements in the synthesis procedure have been discussed in chapter 6.

Chapter 2

Design Of CMOS Op-Amps for Minimum Power and Area

2.1 Introduction

This chapter deals with the design of CMOS op-amps for minimum power and area[1]. As a first step towards the synthesis procedure, the proper representation of the analog circuit (in our case, the op-amp) is very crucial. The hierarchical representation of analog circuits permits the design process to be recast as a sequence of smaller design tasks. Although such a representation makes the synthesis process more tractable, we lose the easy ability to implement design tricks that jumps across many levels of the hierarchy. The choice of the actual representation rests with the designer. The given set of

[1]Power consumed and area of the device are two important parameters which affect the number of functions that can be implemented on a chip. Simultaneous optimization of both will enhance the number of functions implementable on a single chip.

performance specifications is then translated into lower levels of the hierarchy (subblocks), depending on the hierarchical presentation. The process may be repeated inside each subblock. These translated specifications are then used to optimize the part of the circuit at that level of hierarchy, using the optimization routine developed, to meet the overall performance specifications. At the lowest level of the hierarchy, we get sized transistors.

2.2 Synthesis Procedure for a Simple Current Mirror

The current mirrors are frequently used in analog circuits and, in particular, in op-amps. Their design is very crucial for proper performance of the op-amp. For instance, the CMRR and the DC gain of the op-amp are strongly dependent on the quality of the current mirrors. In this section, the details of the synthesis procedure for simple current mirrors are discussed.

Figure 2.1 shows the schematic of a simple current mirror, which uses NMOS devices. The synthesis procedure to minimize the area[2] for a simple current mirror requires the following three performance specifications and three technological parameters.

Performance specifications.

1. Minimum Output Mirror Current I_o^{min},

[2]Throughout out the text, the term area refers to the active area of the circuit. It only includes the sum of the areas of the individual transistors (defined as area = W×L, where W and L are the channel width and length respectively) in the circuit.

2 Minimum Output Resistance R_o^{min}, and

3. Minimum Output Voltage V_o^{min}.

Technological parameters:

1. Device Transconductance Parameter K_n' ($= \mu_n C_{ox}'$, where μ_n is the electron mobility and C_{ox}' is the oxide capacitance per unit area, given by $C_{ox}' = \epsilon_{ox}/t_{ox}$, with ϵ_{ox} and t_{ox} being the oxide relative dielectric permittivity and thickness repectively),

2. Threshold Voltage V_{tn}, and

3. Channel Length Modulation Parameter[3] λ.

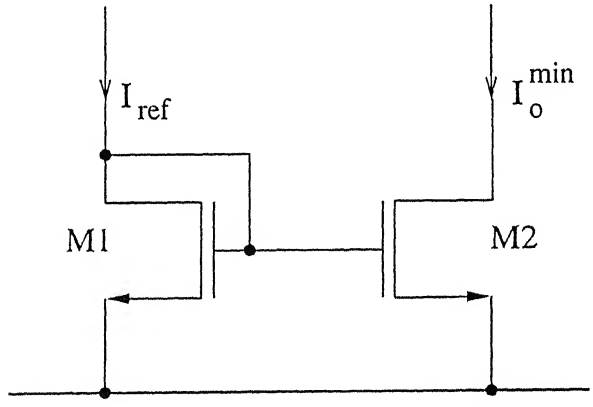


Figure 2.1: The schematic of a simple NMOS current mirror.

It is a well known fact that the channel length modulation parameter λ is a function of the channel length L. Therefore, in our case, where L can take on different values, an accurate model for λ is of crucial importance. In this work, we have developed a model for λ in order to accurately portray its variation with the channel length L.

[3]A model for λ has been developed in Subsection 2.2.1.

2.2.1 Modelling of the Channel-Length Modulation Parameter λ

Biasing of the MOS transistors in the saturation region creates a pinched-off (depletion) region between the drain and the end of the channel. The width of this region, defined as X_d, is a function of V_{DS} and is given by[11]

$$X_d = \sqrt{\frac{2\epsilon_s(V_{DS} - V_{DSat})}{qN_{sub}}}, \tag{2.1}$$

where ϵ_s is the permittivity of S_i, q is the electronic charge, N_{sub} is the substrate doping, V_{DS} is the drain-to-source voltage, and V_{DSat} is the minimum value of V_{DS} for the device to be in saturation.

The effect of this depletion region is to modulate the channel length. The actual effective channel length is given by

$$L_{eff} = L - X_d. \tag{2.2}$$

The channel length modulation parameter λ is given by[11]

$$\lambda = \frac{1}{L_{eff}} \frac{dX_d}{dV_{DS}}. \tag{2.3}$$

Differentiating Eqn.(2.1) with respect to V_{DS}, we get

$$\frac{dX_d}{dV_{DS}} = \frac{K_1}{2} \frac{1}{\sqrt{V_{DS} - V_{DSat}}}, \tag{2.4}$$

where

$$K_1 = \sqrt{2\epsilon_s/(qN_{sub})}. \tag{2.5}$$

From Eqns.(2.3) and (2.4), it is clear that for each value of L, λ would vary with $(V_{DS} - V_{DSat})$. Using the fact that the value of $(V_{DS} - V_{DSat})$ for the current mirror varies between zero and $(V_{DD} - V_{DSat})$, the average value of $(V_{DS} - V_{DSat})$ can be given by

$$K_2 = \frac{V_{DD} - V_{Dsat}}{2} \tag{2.6}$$

In order to model λ appropriately, the choice of the value of $(V_{DS} - V_{DSat})$ is important, which has been replaced by its average value K_2 [Eqn.(2.6)] in this work. Thus, from Eqns.(2.1), (2 2), (2.5), and (2.6), we get

$$L_{eff} \approx L - K_1\sqrt{K_2}, \tag{2.7}$$

and from Eqns.(2.4) and (2.6), we get

$$\frac{dX_d}{dV_{DS}} = \frac{K_1}{2\sqrt{K_2}}. \tag{2.8}$$

Hence, from Eqns.(2.3), (2.7), and (2.8), we get

$$\lambda = \frac{1}{(L - K_1\sqrt{K_2})}\frac{K_1}{2\sqrt{K_2}}, \tag{2.9}$$

or

$$\lambda = \frac{K_1}{2(L\sqrt{K_2} - K_1K_2)}. \tag{2.10}$$

In Eq.(2.10), K_1 and K_2 are both constants for given values of V_{Dsat} and N_{sub}. It is clear from Eq.(2.10) that λ varies inversely with the channel length L. A typical variation of λ with L (for V_{DSat} = 1.5 V and N_{sub} = 1e15 cm^{-3}) is shown in Fig.2.2.

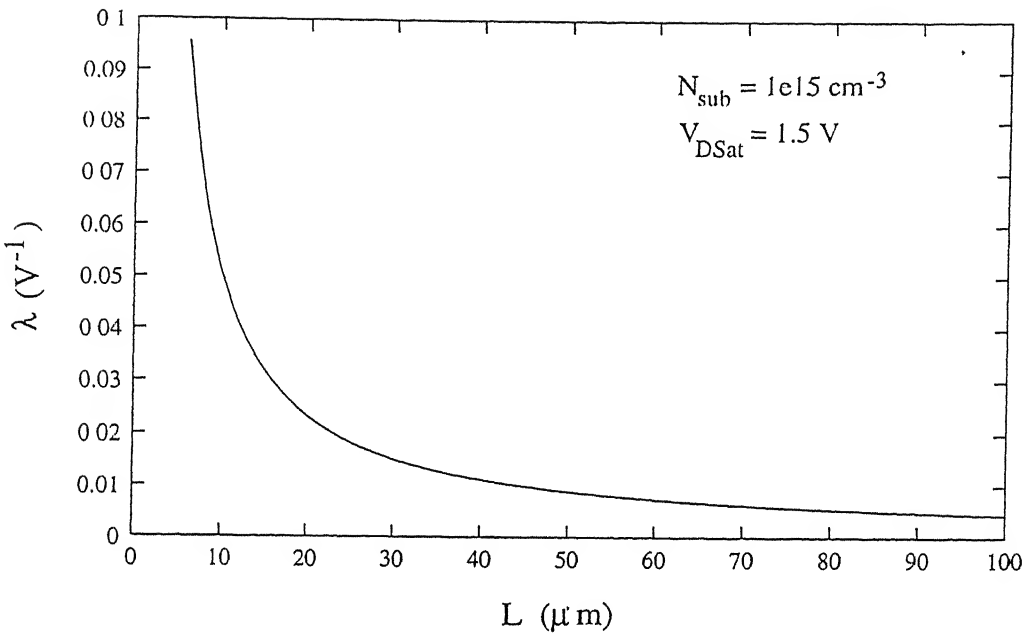


Figure 2.2: The variation of the channel length modulation parameter λ as a function of the channel length L, with $V_{DSat} = 1.5$ V and $N_{sub} = 1e15\ cm^{-3}$.

2.2.2 Constraints

There are two constraints which have been considered in the synthesis procedure carried out in this work. One, we have assumed that the current ratio between the input and the output to be equal to unity (i.e., $I_{ref} = I_o^{min}$). This makes the aspect ratios of M1 and M2 to be equal to each other. Second, we have considered only those values of L and W which fall in between the minimum and the maximum allowable device length (L_{min} and L_{max} respectively) defined by us; which mathematically can be stated as $L_{min} \leq (W, L) \leq L_{max}$. Thus, the values of the aspect ratio (W/L) of the individual transistors are bound in the range of the ratio of the minimum to the maximum allowable device length (i.e., L_{min}/L_{max}) and the ratio of the maximum to the minimum allowable device length (i.e., L_{max}/L_{min}). In other

words, the second constraint limits the search space by restricting the values of the design variables, i.e., the values of W and L for individual transistors The area constraint can be expressed mathematically as $2L_{min}^2 \leq area \leq 2L_{max}^2$. The exact value of the total area taken up by the current mirror is determined by the values of I_o^{min}, R_o, and V_o^{min}.

2.2.3 Optimization Routine for the Simple Current Mirror

For the synthesis procedure of simple current mirrors, the optimization routine, under the constraint of minimizing the area[4] of the current mirror, has been developed in this work. This accepts the three performance specifications and the three technological parameters given earlier, as well as incorporates the variation of λ with L (the model derived in this work). The optimization routine is as follows.

1. Using the fact that $R_o = (\lambda I_o^{min})^{-1}$ and Eqn.(2.10), the values of L required for different values of R_o are obtained. The expression for the output resistance can be given by

$$R_o = \frac{2(L\sqrt{K_2} - K_1 K_2)}{K_1 I_o^{min}} \tag{2.11}$$

[4]The current source is designed to source a certain amount of current, which is evaluated from the performance specifications of the circuit where it is being used. Thus, the optimization routine for the current mirror developed here does not include the constraint of minimum power dissipation, since it is dependent directly on the required value of the bias current.

or[5]

$$2L\sqrt{K_2} = K_1 I_o^{min} R_o + 2K_1 K_2. \tag{2.12}$$

Thus, the required value of L can be obtained from

$$L = \frac{R_o I_o^{min} K_1 + 2K_1 K_2}{2\sqrt{K_2}}. \tag{2.13}$$

2. The value of W is determined by the desired value of the minimum output voltage V_o^{min} ($= V_{GS} - V_{tn}$, where V_{GS} is the applied gate-to source voltage) and using the relation $I_o^{min} = (K'_n/2)(W/L)(V_{GS} - V_{tn})^2$ Thus, the aspect ratio (W/L) of the output transistor M2 can be found from

$$(W/L) = \frac{2I_o^{min}}{K'_n (V_o^{min})^2} \tag{2.14}$$

or

$$W = \frac{2I_o^{min} L}{K'_n (V_o^{min})^2} \tag{2.15}$$

where L is given by Eqn.(2.13).

Thus, the design process is completed for the current mirror.

[5]It is clear from Eqn.(2.11) that output resistance R_o ($= 1/g_d$, where g_d is the drain conductance of the transistor) is a linear function of the channel length L. Thus, the performance of the analog circuits, which is strongly dependent on the output resistance of the transistor, would depend on the channel length L.

2.2.4 Implementation

Based on the constraints and the optimization routine illustrated above, a programme is written in the C-language, which predicts the values of the design variables, i.e , those of W and L. It also calculates the total area taken up by the current mirror. The following values of the performance specifications and technological parameters are used in our optimization routine.

K'_n	:	40 $\mu A/V^2$	V_{tn}	:	1.0 V
I_{ref}	:	40 μA	R_o^{min}	:	1 $M\Omega$
L_{min}	:	1 μm	L_{max}	:	200 μm
V_o^{min}	:	1.5 V	V_{DD}	:	5 V

The aspect ratio (W/L) of M1 (equal to that of M2) and the current flowing through M1 (equal to that of M2) predicted by our optimizer are 16.62 μm/18.70 μm and 40 μA respectively for minimum area ($\approx$ 622 μm^2). These predicted values of the design variables are fed to a SPICE file for cross-verification.

2.2.5 Results and Discussion

Figure 2.3 shows the variation of the output resistance R_o as a function of the channel length L for a bias current of 40 μA, using the model of the channel length modulation parameter λ developed in this work. The result obtained from the SPICE simulation is also shown in the same figure for the sake of comparison. It is obvious from the figure that the results show a very good match between the two. The range of the percent error between our

results and SPICE simulation for R_o over the whole range of the design variable L is 0.57% to 6.13%, which is fairly good. Figure 2.4 shows the variation of the channel width W as a function of the output resistance R_o for a bias current of 40 μA. Figures 2.3 and 2.4 show that both W and L are monotonically increasing functions of R_o.

The area taken up by the current mirror can be expressed mathematically by the following relationship

$$area = 2WL, \tag{2.16}$$

where L and W are given by Eqns.(2.13) and (2.15) respectively. Thus, substituting the expressions for W and L in Eqn.(2.16), we get

$$area = \frac{4I_o^{min}}{K_n'(V_o^{min})^2}\left(\frac{R_o I_o^{min} K_1 + 2K_1K_2}{2\sqrt{K_2}}\right)^2. \tag{2.17}$$

It is clear from Eqn.(2.17) that the area taken up by the current mirror is a quadratic function of R_o for the given values of I_o^{min} and V_o^{min} (K_1 and K_2 are also fixed parameters for a particular process technology), and its variation with respect to R_o is shown in Fig.2.5. Thus, the minimum area of the current mirror is determined by the minimum output resistance R_o^{min}. It is also important to note that the minimum output current is an input to the optimization routine, and, hence, remains the same throughout the range of the output resistance R_o, resulting in no loss of the current carrying capability of the current mirror.

The utility of these data lies in the fact that we can have a range of output resistance at the cost of larger area without losing the current carrying capability of the current mirror, and correspondingly obtain different values of the design variables, i.e., W and L of the individual transistors. In

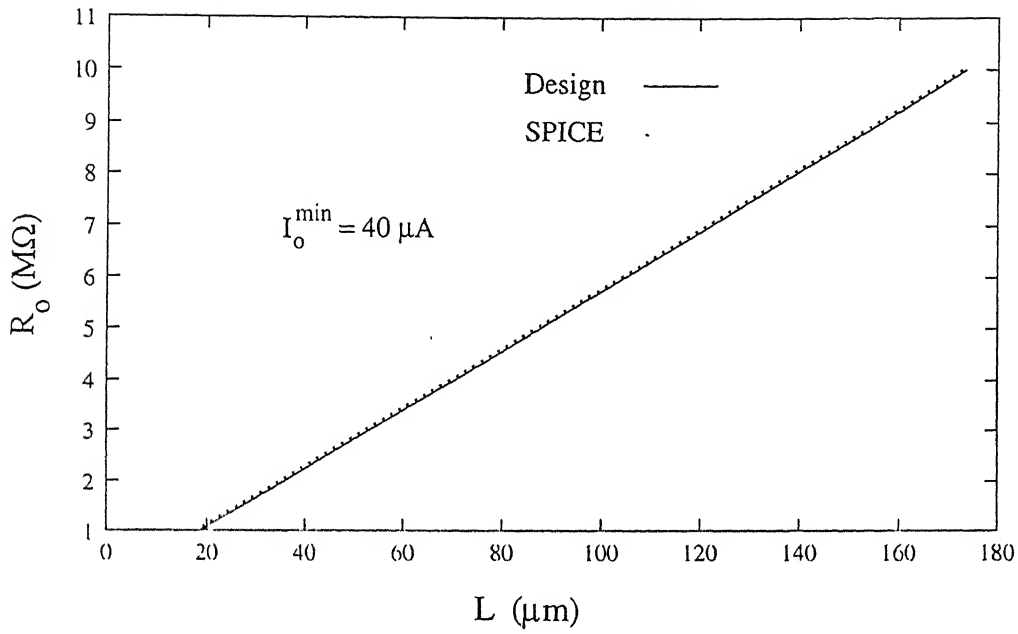


Figure 2.3: The variation of R_o as a function of L, for $I_o^{min} = 40\ \mu A$. The results obtained from the SPICE simulation are also shown for comparison.

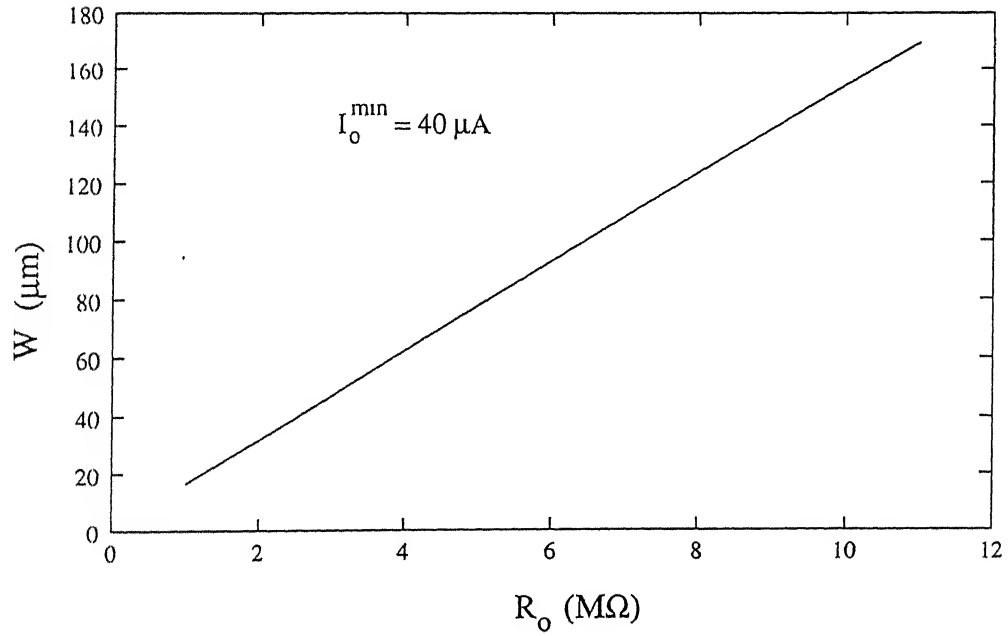


Figure 2.4: The variation of W as a function of R_o, with $I_o^{min} = 40\ \mu A$.

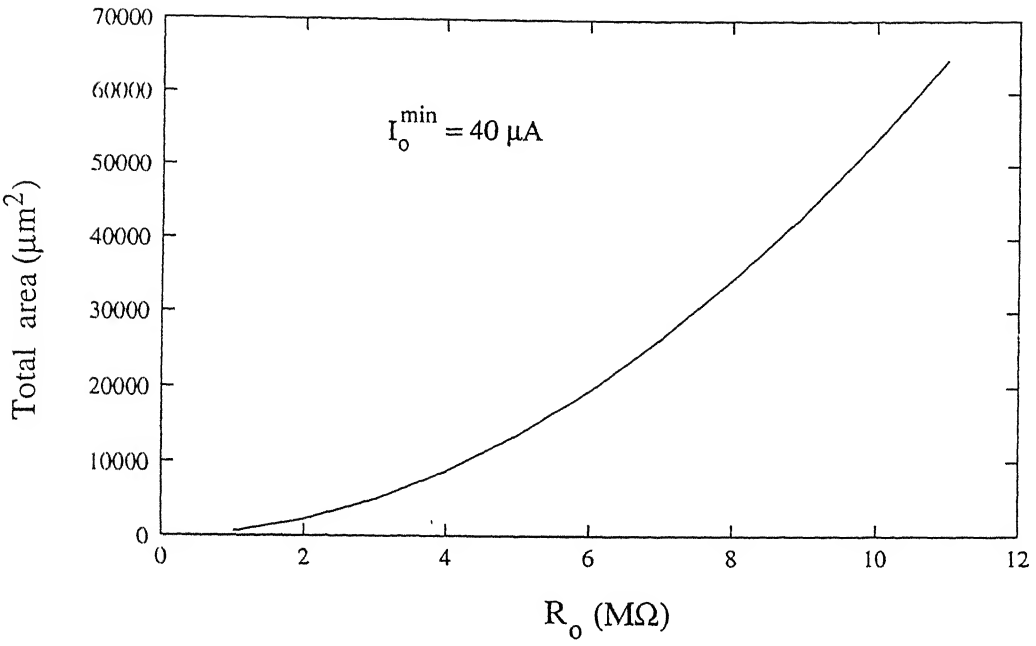


Figure 2.5: The variation of the total area of the current mirror as a function of R_o, with $I_o^{min} = 40\ \mu A$.

other words, these graphs provide the user an easily available reference data for the simple current mirror, optimized for minimum area.

The OASYS [2] provides the optimization routine for minimizing the area of the simple current mirror, where the expression for the output impedance used is $R_o = (\lambda I_o^{min})^{-1}(L/L_{min})$. A closer look at this equation tells us that R_o is a quadratic function of L, instead of being a linear function, which has been verified in this work. Based on the optimization routine given in OASYS, we have designed and verified (using SPICE) the characteristics for the simple current mirror. The range of the percent error between OASYS results and SPICE simulation for R_o over the whole range of the design variable L is between 74.07% and 92.19%. This is alarmingly high, which prompted us to develop our own optimization routine, the result of which is far better than

that predicted by OASYS.

It is important to note here that the most widely used op-amp topologies make use of the simple current mirror block as the biasing element. This led us to consider the synthesis procedure for this block only, which not only provides good results (when compared with SPICE simulations), but also the idea is extendable to other widely used current sources, e.g., the cascode current source and the Wilson current source, with proper modifications. Further, such work on current mirrors would build a sound foundation for the development of the cell libraries for various types of current mirrors in near future.

2.3 The Synthesis Procedure for Op-Amps

A typical block diagram of a symmetric CMOS op-amp, consisting of the differential pair, the current mirror, the output bias, the differential-pair bias, and driving a capacitive load C_L, is shown in Fig.2.6. We are provided with the following six input performance specifications and three technological parameters in order to design the op-amp for minimum power and area.

Performance specifications:

1. Slew Rate SR,
2. Load Capacitance C_L,
3. Unity Gain Frequency f_c,
4. DC Open Loop Gain A_{v0},

5. Maximum Output Voltage V_{o-OA}^{max} [6], and

6. Minimum Output Voltage V_{o-OA}^{min}.

Technological parameters:

1. Device Transconductance Parameters K_n' and K_p' ($= \mu_p C_{ox}'$, where μ_p is the hole mobility),

2. Threshold Voltages V_{tn} and V_{tp}, and

3. Channel Length Modulation Parameter λ.

2.3.1 Constraints

In this design of the op-amp, its minimum power consumption is decided by the desired values of the slew rate and the load capacitance. The second constraint, considered for the synthesis procedure for the simple current mirror in order to minimize its total area, has also been considered here for the synthesis procedure for the op-amp in order to minimize its total area. Besides this, the search space is further restricted by the fact that only those values of α (defined later in Subsection 2.3.2) are permissible for which the above constraint is fulfilled for the current mirror subblock and the output bias subblock simultaneously. It is important to note that for a given combination of the slew rate and the load capacitance, the power and the area are minimized more or less independently. In other words, first the minimum value of the bias current I_{Bias} is determined from the required value of the slew rate, hence,

[6] The "OA" subscript denotes op-amp.

completing the power minimization part. Then, for the determined value of the bias current, the area minimization is done.

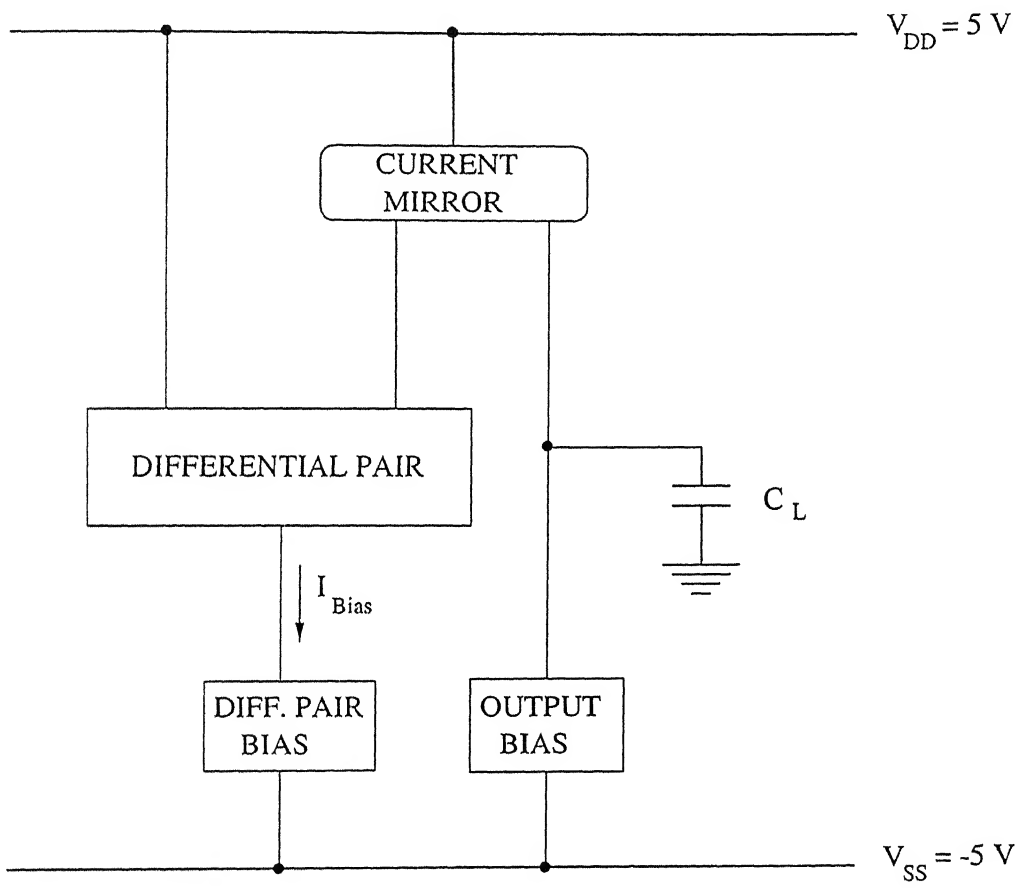


Figure 2.6: The block diagram of a symmetric CMOS op-amp.

2.3.2 Optimization Routine

In the synthesis procedure for the op-amp considered, the optimization routine to minimize its power and area has been developed. The various steps of the routine are as follows.

1. The bias current I_{Bias} is chosen to achieve the desired slew rate, using the fact that $SR \leq (I_{Bias}/C_L)$, and, at the very first step, the power is minimized by choosing the smallest possible value of the bias current, given by

$$I_{Bias} = C_L \times SR. \tag{2.18}$$

2. The choice of the transconductance (G_m) of the differential pair subblock is decided by the fact that $f_c = G_m/(2\pi C_L)$. The relation $G_m = \sqrt{K'_n(W/L)_i I_{Bias}}$ is used to design this subblock, where $(W/L)_i$ is the aspect ratio of the input transistors used in that subblock. The value of $(W/L)_i$ of the input transistors used in this subblock can thus be given by

$$(W/L)_i = \frac{G_m^2}{K'_n I_{Bias}}. \tag{2.19}$$

3. A parameter α is now defined, where $r_{o-M} = \alpha r_{o-B}$, and r_{o-M} and r_{o-B} are the output resistances of the current mirror and the output bias subblocks respectively.

4. Using the fact that $A_{v0} = G_m(r_{o-M} \| r_{o-B})$, we get

$$r_{o-M} = \alpha r_{o-B} = (A_{v0}/G_m)(1+\alpha). \tag{2.20}$$

5. For different values of α, the current mirror subblock is designed using the following input specifications as described in Section 2.2.
   Minimum Output Mirror Current, $I_{o-M}^{min} = I_{Bias}/2$
   Output Resistance, $R_o = r_{o-M} = (\lambda I_{o-M}^{min})^{-1}$
   Minimum Drain-to-Source Voltage, $V_{o-M}^{min} = V_{DD} - V_{o-OA}^{max}$.

6. For different values of α, the output bias subblock is designed using the following input specifications as described in Section 2.2.
   Minimum Output Bias Current, $I_{o-B}^{min} = I_{Bias}/2$

Output Resistance, $R_o = r_{o-B} = (\lambda I_{o-B}^{min})^{-1}$

Minimum Drain-to-Source Voltage, $V_{o-B}^{min} = V_{o-OA}^{min} - V_{SS}$.

7. The relation $I_{Bias} = (K_n'/2)(W/L)_{DB}(V_{Bias} - V_{SS} - V_{tn})^2$ is used to design the differential-pair bias subblock, where $(W/L)_{DB}$ is the aspect ratio of the individual transistors used in that particular subblock. For a chosen value of the aspect ratio $[(W/L)_{DB}]$ of the transistors used, V_{Bias} is given by

$$V_{Bias} = \sqrt{2I_{Bias}/(K_n'(W/L)_{DB})} + V_{SS} + V_{tn}. \tag{2.21}$$

2.3.3 Implementation

Based on the optimization routine and the constraints, a programme written in the C-language predicts the values of the design variables, i.e., W and L of the individual transistors and the bias current. It also calculates the total area of all the transistors. These values of the design variables are fed to a SPICE file for cross verification, which uses the symmetric CMOS op-amp, as shown in Fig.2.7, where transistors M1 and M2, M4 and M6, M7 and M8, and M9 and M10 form the differential pair subblock, the current mirror subblock, the output bias subblock, and the differential-pair bias subblock respectively. The input specifications for A_{v0}, f_c, and SR used in this design of the op-amp are 40 dB, 1 MHz, and 2 V/μsec respectively.

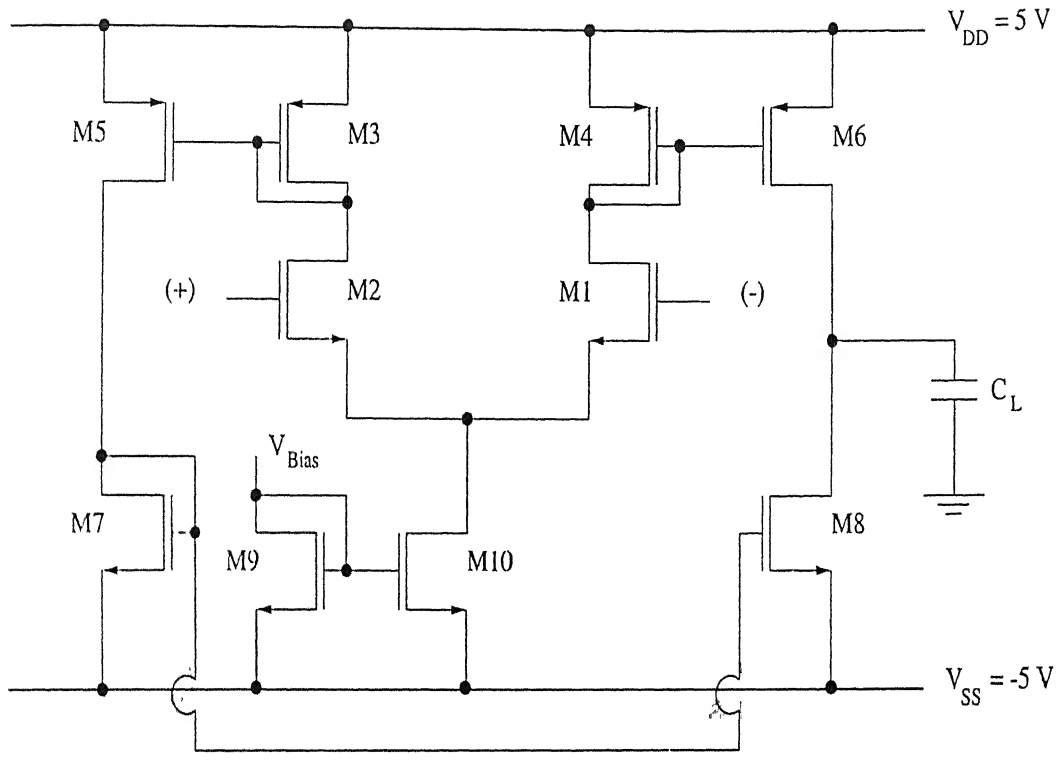


Figure 2.7: The detailed circuit diagram of the symmetric CMOS op-amp considered in this work.

The values of the parameters used are as follows.

K_n'	:	40 $\mu A/V^2$	K_p'	:	20 $\mu A/V^2$
V_{tn}	:	1 V	V_{tp}	:	-1 V
L_{min}	:	1 μm	L_{max}	:	200 μm
V_{o-OA}^{max}	:	4.0 V	V_{o-OA}^{min}	:	-4.0 V
C_L	:	5 pF			

From the optimizer, a typical set of the values of the design variables for minimum power ($\approx$ 200 μW) and minimum area ($\approx$ 125 μm^2) are obtained. These values of the design variables are shown in Table 2.1 and are used for SPICE simulations.

Table 2.1: A typical set of the values of the design variables obtained from our optimizer for minimum power ($\approx$ 200 μW) and minimum area ($\approx$ 125 μm^2), which are used for the SPICE simulations.

Transistors	W/L μm/μm	Current through transistor (μA)
M1, M2	2.40/1.00	5.0
M3, M4	2.07/4.15	5.0
M5, M6	2.07/4.15	5.0
M7, M8	2.50/1.00	5.0
M9, M10	1.00/2.00	10.0

2.3.4 Results and Discussion

Figures 2.8 and 2.9 show the variations of W and L with α respectively for the current mirror subblock. According to Eqns.(2.13) and (2.20), r_{o-M} is a linear function of both L and α. Thus, L would vary linearly with α, which has been substantiated in Fig.2.9. Since the aspect ratio remains the same (for constant current drive), W also becomes a linear function of α. On the other hand, r_{o-B} varies inversely with α according to Eqn.(2.20). This makes L, as well as W, to vary inversely with α. These variations of W and L with respect to α are shown in Figs.2.10 and 2.11 respectively for the output bias subblock.

Figure 2.12 shows the variation of the total area for the sym-

metric CMOS op-amp with respect to α. It can clearly be seen from Fig.2.12 that the lowest value of the total area occurs for the value of α in the vicinity of 1.4. It has been observed that different combinations of the slew rate and the load capacitance values, giving rise to different minimized values of the dissipated power, alter the corresponding values of α, as well as the minimum values of the area.

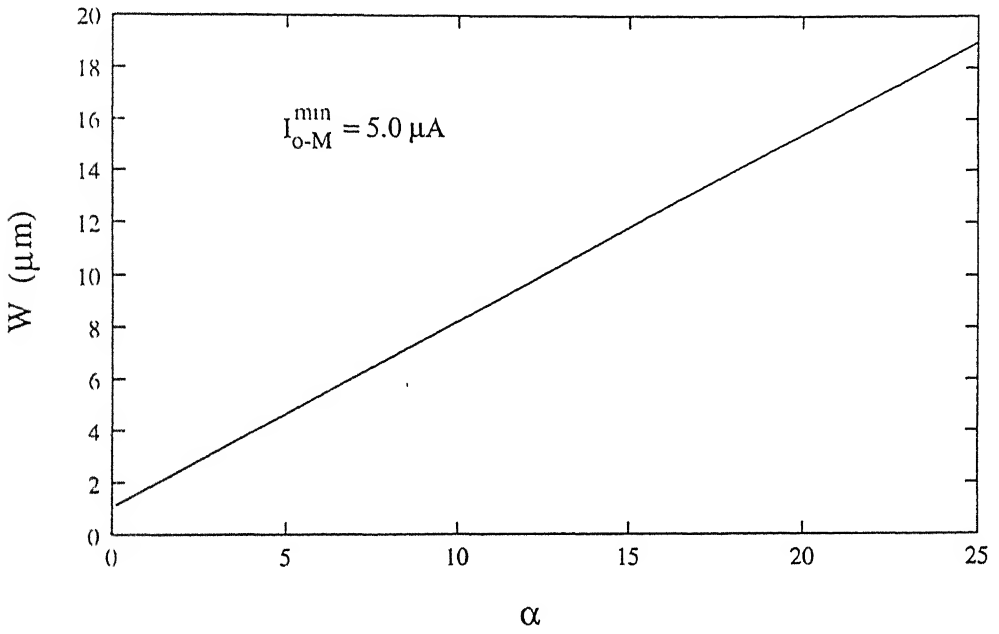


Figure 2.8: The variation of W with α (for the current mirror subblock).

The results obtained from the SPICE simulation is in full agreement with the result obtained from our design, which has been verified over the entire range of the design variables. Table 2.2 shows a comparison between the results obtained from our design and the SPICE simulation for a particular set of performance specifications.

Figures 2.13 and 2.14 show the gain plot and the phase plot respectively, highlighting the gain margin and the phase margin obtained from

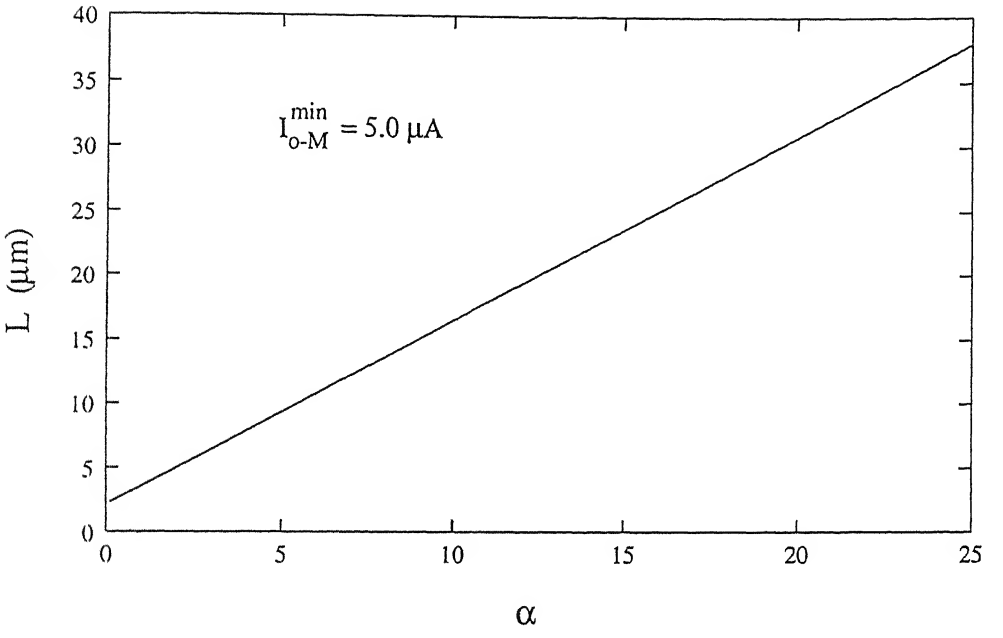


Figure 2.9: The variation of L with α (for the current mirror subblock).

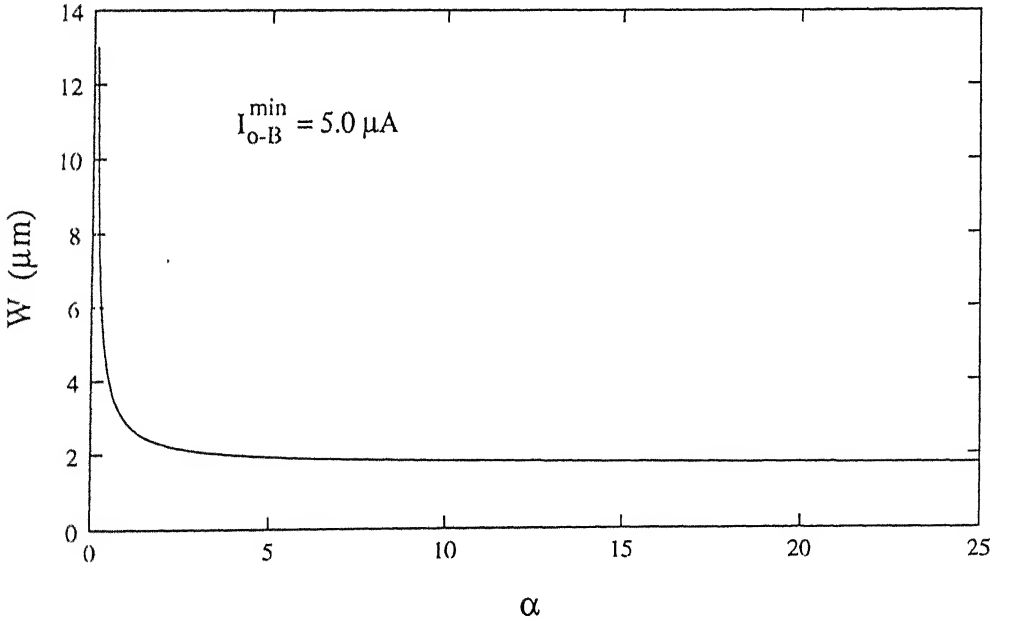


Figure 2.10: The variation of W with α (for the output bias subblock).

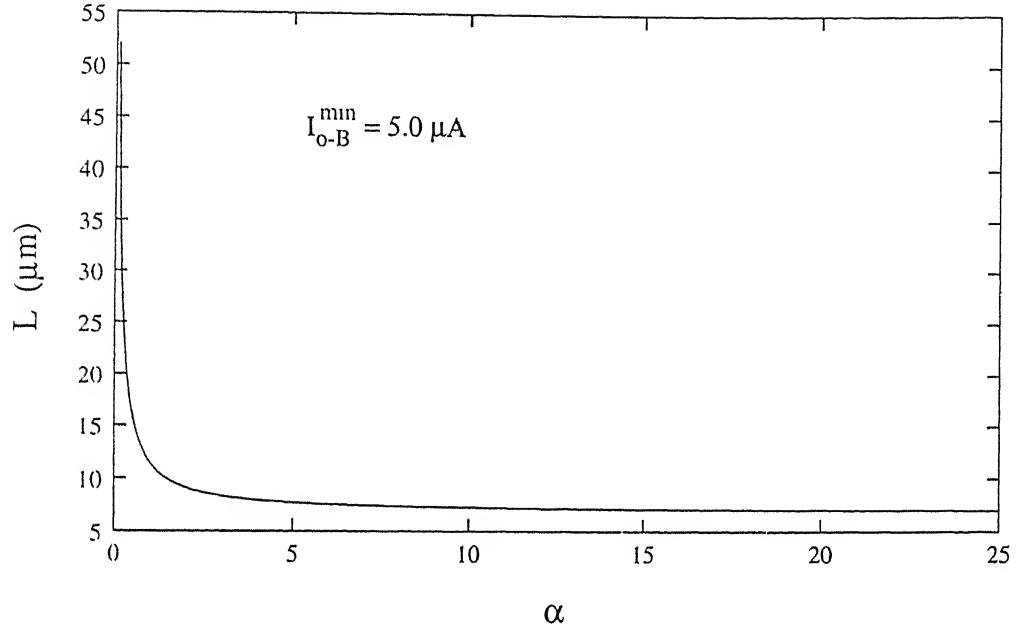


Figure 2.11: The variation of L with α (for the output bias subblock).

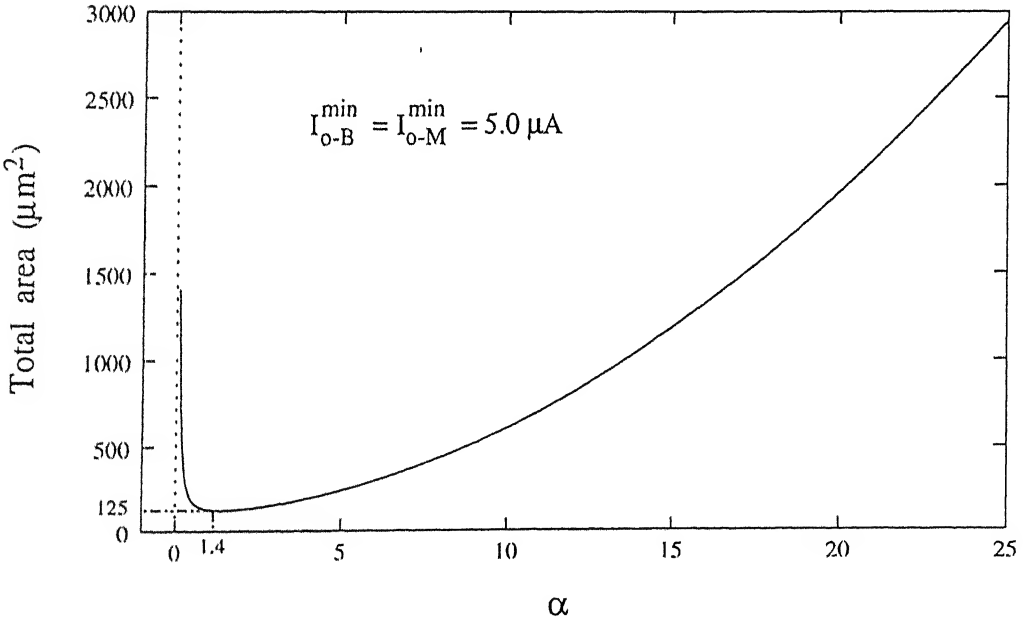


Figure 2.12: The variation of the total area with α.

Table 2.2. The comparison of the results obtained from our design and the SPICE simulation.

Specs.	Design	SPICE
A_{vo} (dB)	40	40.05
f_c (MHz)	1 0	1.07
SR (V/μsec)	2.0	1.98

the design. These two plots have been obtained for the design variables corresponding to the minimum area ($\approx$ 125 μm^2) and the minimum power ($\approx$ 200 μW). Since the system has a large negative gain margin ($\approx$ -52 dB) and a large phase margin ($\approx 88^o$), it would have a superior stability.

2.3.5 The Second Order Effects

The DC open-loop gain of the symmetric CMOS op-amp is comparatively less as compared to the conventional 2-stage CMOS op-amp topology. This is because of the fact that only the second stage is contributing to the total gain. The overall gain can be made to go up by removing the connection between the gate and the drain of M4, and by connecting a battery source of suitable value to the gate of M4 in order to bias the transistors properly. This makes both the stages to contribute to the total gain, resulting in a higher gain, and, hence, higher unity gain frequency. The SPICE simulation for the symmetric CMOS op-amp, with the modifications illustrated above, shows an increase in the DC open-loop gain and in the unity gain frequency - a fact that can be verified analytically. For the simulation by SPICE, no compensating capacitor has been used, and all the parameters and the design variables used

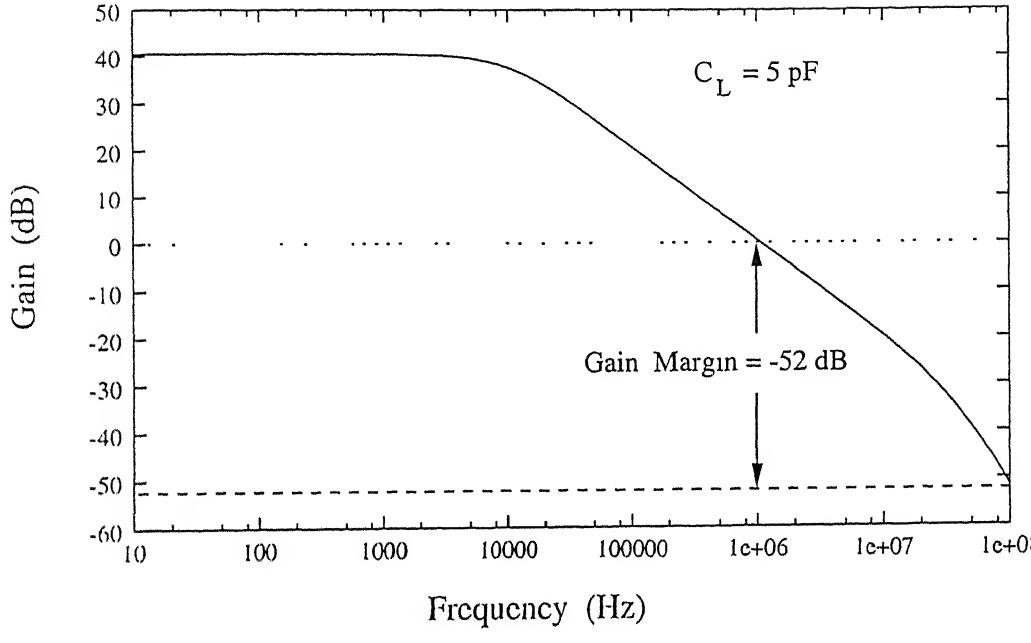


Figure 2.13: The gain versus frequency plot of the symmetric CMOS op-amp obtained using the optimized values of the aspect ratios of the transistors under the constraints of minimum power ($\approx 200\ \mu W$) and minimum area ($\approx 125\ \mu m^2$).

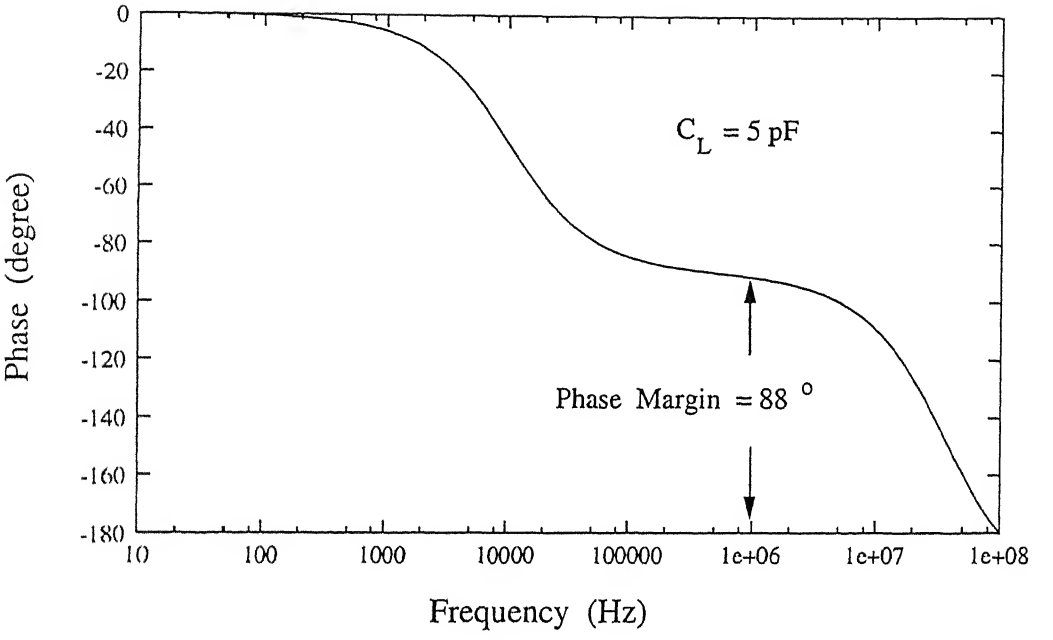


Figure 2.14: The phase versus frequency plot of the symmetric CMOS op-amp obtained using the optimized values of the aspect ratios of the transistors under the constraints of minimum power ($\approx$ 200 μW) and minimum area ($\approx$ 125 μm^2).

to obtain the results shown in Figs.2.13 and 2.14 are used. The results obtained for this improved stage are as follows.

A_{vo}	$\approx$	75 dB
f_c	$\approx$	5.01 MHz
Phase Margin	$\approx$	8^o
Gain Margin	$\approx$	-37 dB

The simulation shows a poor phase margin of only 8^o. If a compensating capacitor of value equal to the value of the load capacitance (C_L = 5 pF) is used, it enhances the phase margin to 50°, and thus renders better stability to the system.

In almost all kinds of circuit applications, the demand for minimum power and area is becoming extremely crucial (since it affects the packing density and the cost per function in an IC chip), making it inevitable for circuit designers to incorporate this factor in circuits designed for a particular set of performance specifications. Our synthesis approach for a particular configuration of the CMOS op-amp (i.e., the symmetric structure) for minimum power and area provides reasonably good results, when compared with SPICE simulations. This is a good example which shows how a given set of performance specifications for the op-amp can be met by designing its various subblocks in an analytical manner. This approach, with slight modifications (which would depend upon the set of performance specifications and the behavioural model of the circuit), may be extended to other CMOS op-amp topologies. Besides this, it may find its use in the design of op-amps for a wide variety of specifications appropriate for complex analog systems (e.g., high gain, high bandwidth, high slew rate, etc.).

In the next three chapters, the design and optimization procedures for CMOS op-amps under the constraints of high bandwidth (or high unity gain frequency), high gain and high unity gain frequency, and high slew rate are presented.

Chapter 3

Design Of CMOS Op-Amps for High Bandwidth

3.1 Introduction

This chapter deals with the design aspects of CMOS op-amps for high bandwidth (or high unity gain frequency). In the process of analog synthesis, proper mathematical representation of the analog circuit (in our case, the op-amp) is very crucial. Such a representation is based on the set of performance specifications and the behaviour of the circuit. The bandwidth of the op-amp is a high frequency parameter, therefore, the effect of the capacitances appearing at the various nodes (which are of the order of pF) needs to be incorporated into the small-signal model in order to accurately represent the op-amp for high frequency operation. While designing a CMOS op-amp for high bandwidth, the designer has to keep the phase margin sufficiently

high for better stability of the op-amp, which again depends on the various capacitances appearing at the various nodes.

3.2 Synthesis Procedure for a CMOS op-amp

In this design of CMOS op-amps for high bandwidth, we have considered a single stage configuration, as shown in Fig.3.1. In this structure, there are three nodes (3, 4, and 5), which play crucial roles in the determination of the positions of the poles. The detailed analysis is discussed in Subsection 3.2.2.

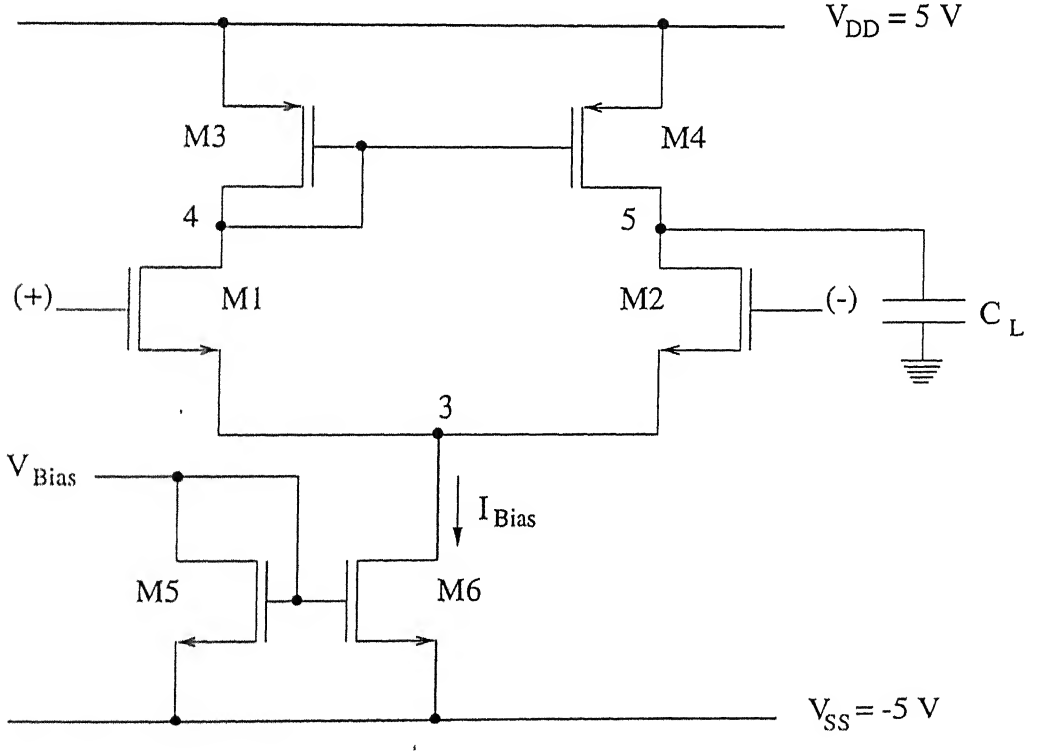


Figure 3.1: The schematic of a simple single-stage CMOS op-amp.

3.2.1 Input Specifications

The following input specifications are used:

1. the load capacitance C_L,
2. the device transconductance parameters K'_n and K'_p,
3. the threshold voltages V_{tn} and V_{tp},
4. the gate-to-drain capacitance C_{GD}, the drain to body capacitance C_{DB}, and the gate-to-source capacitance C_{GS}[1], and
5. the channel length modulation parameter λ.

3.2.2 Mathematical Representation

The resistance (R_{n4}) at node 4 with respect to ground is given by

$$R_{n4} = r_{o1} \| 1/g_{m3}, \tag{3.1}$$

or

$$R_{n4} \approx 1/g_{m3}, \tag{3.2}$$

as $r_{o1} >> 1/g_{m3}$.

The resistance (R_{n5}) at node 5, which is the output node, with respect ground is given by

$$R_{n5} = R_{OUT} = r_{o2} \| r_{o4} = r_{o2}/2. \tag{3.3}$$

[1] C_{SB} has no role to play as individual transistor's body and source are tied together in CMOS.

The resistance (R_{n3}) at node 3 is given by $1/2g_{m1}$ (when looking up) and r_{o6} (when looking down)[2]. For differential gain, unity gain frequency, and slew rate considerations, it (i.e., R_{n3}) does not play any role. It is useful for common mode considerations.

It is clear from Eqns.(3.2) and (3.3) that $R_{n5} >> R_{n4}$. Besides, the load capacitance C_L appears at node 5. The device capacitances appearing at the nodes are generally of the order of 1 pF or less, whereas the load capacitance is normally in the range of 1 to 20 pF. Thus, the values of R_{n5} and R_{n4}, and the values of the corresponding capacitances appearing at nodes 5 and 4 (the value of the capacitance at node 5 would be greater than that at node 4) would make sure that the dominant pole would occur at node 5, whereas the non-dominant pole at node 4.

Thus, it can concluded that although the system (as shown in Fig.3.1) has three nodes (3, 4, and 5), the poles contributed only by the two nodes (4 and 5) are of any importance. In other words, we basically have a two pole system, out of which one is dominant (at node 5) and the other is non-dominant (at node 4).

The -3 dB cutoff frequency or the dominant pole frequency f_d, created on node 5, is given by

$$f_d = \frac{1}{2\pi R_{n5}(C_{n5} + C_L)}, \tag{3.4}$$

where $C_{n5} = C_{GD4} + C_{DB4} + C_{GD2} + C_{DB2}$. The capacitances C_{GD4} and C_{DB4} are connected to the drain of M4; and C_{GD2} and C_{DB2} are connected to the drain of M2.

[2] r_{o6} affects the DC open loop-gain, however, this affect is not appreciable as $g_m >> g_d$.

The unity gain frequency f_c is given by

$$f_c = A_v f_d, \tag{3.5}$$

where

$$A_v = g_{m1} R_{OUT}. \tag{3.6}$$

Thus,

$$f_c = \frac{g_{m1}}{2\pi(C_{n5} + C_L)}. \tag{3.7}$$

It is clear from Eqn.(3.7) that for a given value of the load capacitance, the unity gain frequency is determined by the transconductance parameter of the input transistors g_{m1}, which can be set by choosing I_{Bias} and the aspect ratio of the input transistors $(W/L)_1$.

The non-dominant pole f_{nd} is created at node 4, and is given by

$$f_{nd} = \frac{1}{2\pi R_{n4} C_{n4}}, \tag{3.8}$$

where $C_{n4} = C_{GD1} + C_{DB1} + C_{DB3} + C_{GS3} + C_{GS4} + C_{GD4}$. The capacitance C_{GD4} is connected to the drain of M4; C_{GD1} and C_{DB1} are connected to the drain of M1; C_{GS3} and C_{GS4} are connected to the gates M3 and M4, and C_{DB3} is connected to the drain of M3.

The phase margin, an important parameter for stability considerations, is determined by the positions of the dominant and the non-dominant poles. For sufficient phase margin, f_{nd} should be equal to f_d [12]. This can be used to relate the aspect ratio $[(W/L)_4]$ of the load transistors with that of

the input transistors $[(W/L)_1]$. Therefore,

$$\frac{g_{m3}}{C_{n4}} = \frac{g_{m1}}{C_{n5} + C_L}, \tag{3.9}$$

or

$$(W/L)_4 = \frac{K'_n}{K'_p}(W/L)_1(\frac{C_{n4}}{(C_{n5} + C_L)})^2. \tag{3.10}$$

3.2.3 Optimization Routine

In order to analyse the variation of the unity gain frequency f_c and maximize it with respect to the aspect ratio of the input transistors $(W/L)_1$ for a given value of the bias current I_{Bias}, we have developed an optimization routine based on the mathematical representation, as illustrated in Subsection 3.2.2. The various steps of the optimization routine are given below.

1. The value of the bias current I_{Bias} ($\leq$ 1 mA) is chosen[3].

2. For a chosen value of I_{Bias}, f_c is obtained as a function of the aspect ratio of the input transistors $[(W/L)_1]$ by using Eqn.(3.7) and substituting for the expression of g_m. Thus,

$$f_c = \frac{\sqrt{K'_n I_{Bias}}}{2\pi(C_{n5} + C_L)}\sqrt{(W/L)_1}. \tag{3.11}$$

3. For a given value of $(W/L)_1$, the value of $(W/L)_4$ is obtained from Eqn.(3.10).

[3]Since the current level in MOS is the order of hundreds of μA, we have kept $I_{Bias} \leq 1$ mA.

4. For a chosen value of the aspect ratio of the transistors used in the differential-pair bias subblock $(W/L)_5$ $(= (W/L)_6)$, the value of V_{Bias} is obtained from Eqn.(2.21).

3.2.4 Implementation

The value of the aspect ratio $(W/L)_1$ of the input transistors, which lies in the range of 1 and 100, determines the area constraint, whereas the constraint of power consumption is determined by the fact that I_{Bias} should be less than 1 mA

Based on the design plan, a programme is written in the C-language, which predicts the variation of f_c with the aspect ratio of the input transistors $[(W/L)_1]$ for a given value of I_{Bias} . This also predicts the values of $(W/L)_4$, V_{Bias}, and the total area of the op-amp. These values are fed to a SPICE file for cross-verification of the design. The following parameters have been used.

K'_n	:	82 $\mu A/V^2$	K'_p	:	41 $\mu A/V^2$
V_{tn}	:	0.7 V	V_{tp}	:	-0.8 V
I_{Bias}	:	10, 100, 1000 μA	λ	:	0.01 V^{-1}
C_{BD}	:	0.75 pF	C_{GDO}	:	0.15 pF
V_{Bias}	:	-3.950 V (for $I_{Bias} = 100$ μA)	C_{GSO}	:	0.1 pF
C_L	:	5 pF			

A typical set of values of the aspect ratios and the currents through the respective transistors obtained from our optimizer and used for SPICE simulation is shown in Table 3.1.

Table 3.1: A typical set of the values of the aspect ratios and the currents through respective transistors obtained from our optimizer and used for SPICE simulation.

Transistor	W/L (μm/μm)	Current through transistor (μA)
M1, M2	20 0/1.0	50
M3, M4	3.26/1.0	50
M5, M6	20.0 /1.0	100

3.2.5 Results and Discussion

It is clear from Eqn.(3.11) that f_c would vary as the square-root of the aspect ratio of the input transistors $[(W/L)_1]$ for given values of the bias current I_{Bias} and the load capacitance C_L. Figure 3.2 shows the variation of f_c with the aspect ratio of the input transistors $[(W/L)_1]$ for different values of I_{Bias} (10, 100, and 1000 μA).

Equation (3.10) relates the aspect ratio of the input transistors $[(W/L)_1]$ and the aspect ratio of the load transistors $[(W/L)_4]$. Figure 3.3 shows the variation of $(W/L)_4$ with $(W/L)_1$. It is clear from Eqn.(3.10) that the relation between $(W/L)_4$ and $(W/L)_1$ is independent of the bias current. Thus, it can be inferred that for the same value of $(W/L)_1$, different values of f_c can be obtained independently for different values of I_{Bias}. Figure 3.4 shows the variation of the total area of the op-amp with f_c for different values of the bias current I_{Bias} (10, 100, and 1000 μA). It can be inferred that the same value of f_c can be obtained at either higher (lower) value of I_{Bias} with

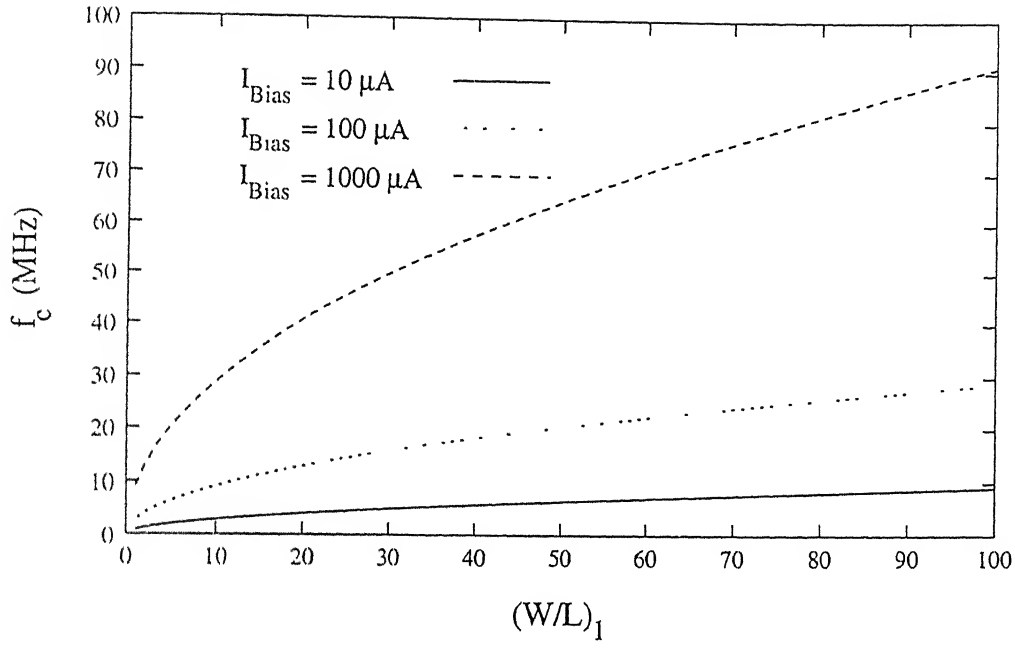


Figure 3.2: The variation of f_c with the aspect ratio of the input transistors $(W/L)_1$ for different values of I_{Bias} (10, 100, and 1000 μA).

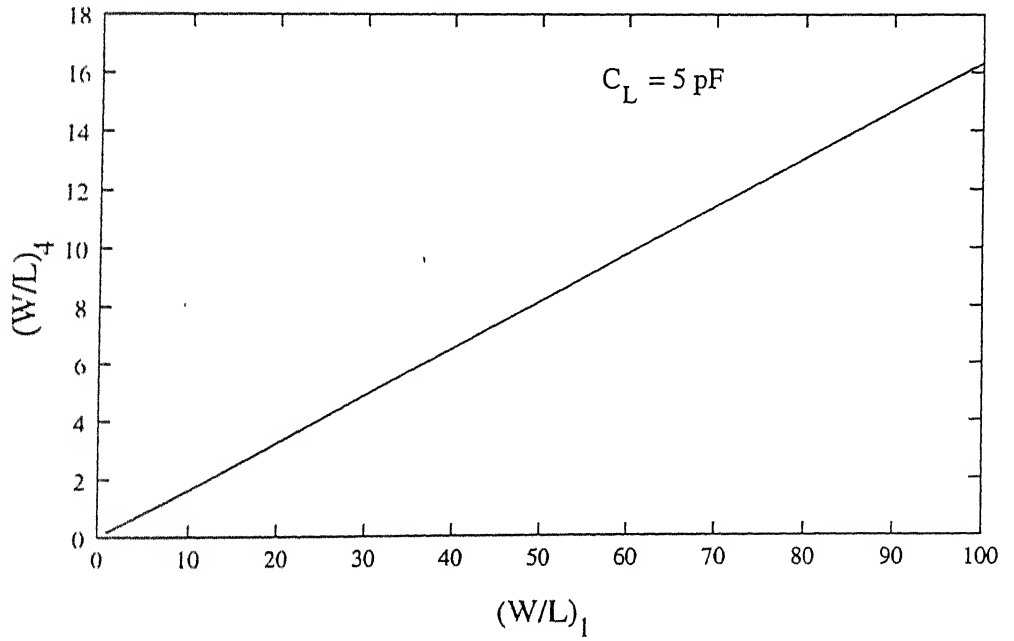


Figure 3.3: The variation of the aspect ratio of the load transistors $(W/L)_4$ with the aspect ratio of the input transistors $(W/L)_1$.

correspondingly lower (higher) value of the total area.

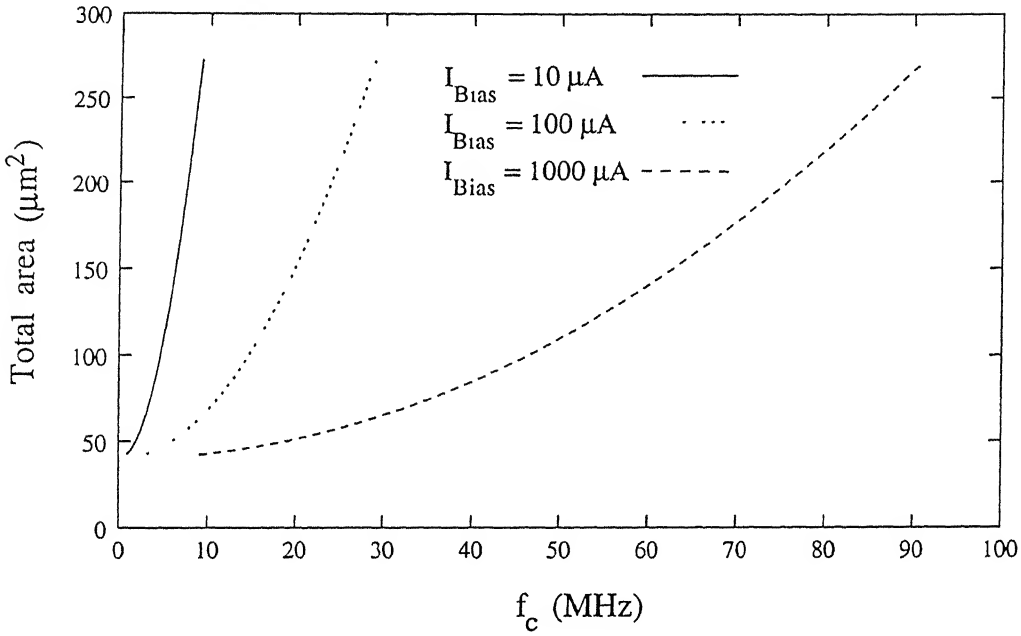


Figure 3.4: The variation of the total area with f_c for different values of I_{Bias} (10, 100, and 1000 μA).

The SPICE simulation of our design shows reasonably good match with the results obtained from our optimizer, which has been done over the entire range of the aspect ratio of the input transistors $(W/L)_1$ and for different values of the bias current I_{Bias} (10, 100, and 1000 μA). Figures 3.5 and 3.6 show the gain plot and the phase plot respectively obtained from SPICE simulation for the values of the aspect ratios and the currents listed in Table 3.1. The comparison of the results obtained from the design and the SPICE simulation are shown in Table 3.2.

Table 3.2: The comparison of the results obtained from our design and SPICE simulation.

Specs.	Design	SPICE
f_c (MHz)	11.8	11.2

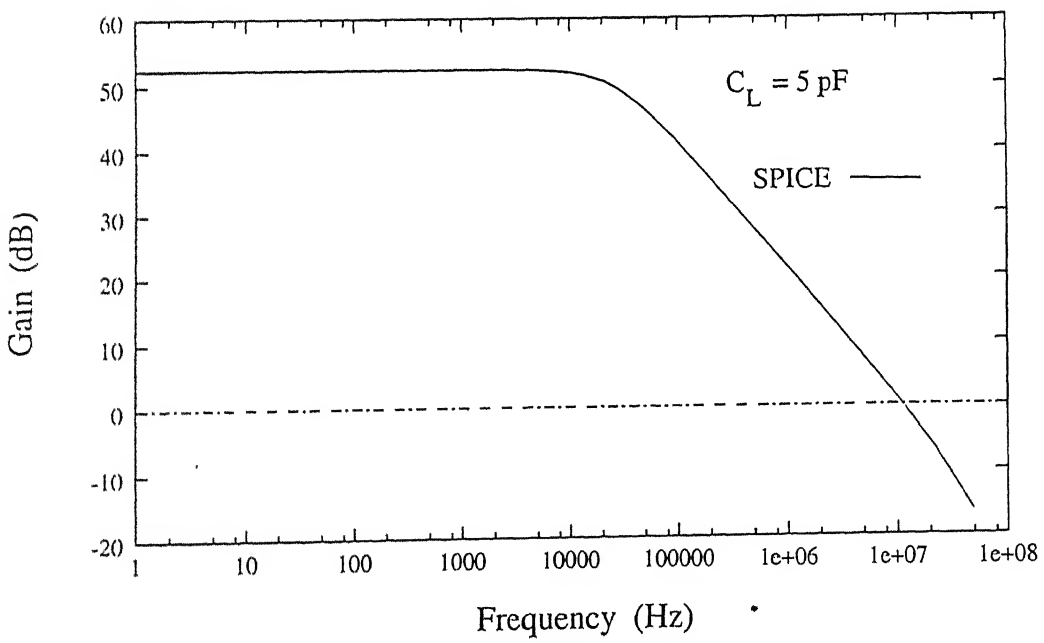


Figure 3.5: The gain versus frequency plot obtained for the aspect ratios and the currents through the respective transistors listed in Table 3.1, as obtained from SPICE simulations.

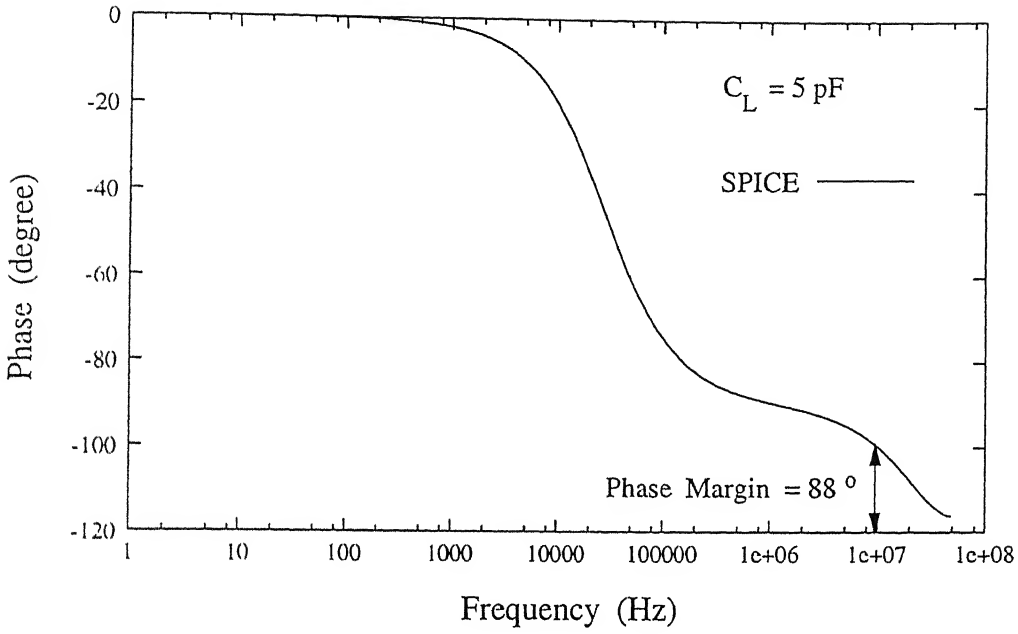


Figure 3.6: The phase versus frequency plot obtained for the aspect ratios and the currents through the respective transistors listed in Table 3.1, as obtained from SPICE simulations.

From Figs.3.2 and 3.4, it can be inferred that unlimited values of f_c can be obtained at the higher cost of either power or area or both. In this design of the op-amp for high bandwidth, we have assumed that the node capacitances C_{n4} and C_{n5} are independent of the sizes of the transistors connected to the respective nodes. This is not the case, however. The larger the aspect ratios, the larger the node capacitances are. Thus, we can not have unlimited values of f_c. So contrary to what Figs.3.2 and 3.4 suggest, after a certain value of the aspect ratio of the input transistors $(W/L)_1$, the value of f_c actually starts falling.

3.2.6 The Capacitance Model

A model is required in order to link the values of the node capacitances to the transistor sizes. After a certain size, the capacitances grows linearly with the aspect ratios of the transistors. The node capacitances C_n are modelled as given by [12]

$$C_n = C_{n0} + k\frac{W}{L}, \tag{3.12}$$

where $C_{n0} = 0.5$ pF, and k = 0.1 pF.

3.2.7 Optimization Routine Based on Capacitor Model

Based on the capacitor model illustrated above, the optimization routine can be developed in order to maximize (or optimize) f_c, which is the modified form of the optimization routine illustrated in Subsection 3.2.3. The various steps of the routine are as follows.

1. Using Eqn.(3.11) and the capacitor model [Eqn.(3.12)], f_c can be expressed as

$$f_c = \frac{\sqrt{K_n' I_{Bias}}}{2\pi} \frac{\sqrt{(W/L)_1}}{C_{n0} + C_L + k((W/L)_1 + (W/L)_4)}. \tag{3.13}$$

2. Using Eqn.(3.10) and the capacitor model, $(W/L)_4$ can be expressed as

$$(W/L)_4 = \frac{K_n'}{K_p'}(W/L)_1 \left(\frac{C_{n0} + k((W/L)_1 + (W/L)_4)}{(C_{n0} + C_L + k((W/L)_1 + (W/L)_4))}\right)^2. \tag{3.14}$$

3. For a chosen value of the aspect ratio of M5 (or M6), the value of V_{Bias} is given by Eqn.(2.21).

3.2.8 Implementation

Based on the above optimization routine, a programme is written in the C-language in order to predict the variation of f_c with the aspect ratio of the input transistors. It also calculates $(W/L)_4$ and corresponding values of the node capacitances. It is clear from Eqn.(3.14) that for each value of $(W/L)_1$, we have a cubic equation in $(W/L)_4$. The meaningful solution of this equation (explained later) and the corresponding value of $(W/L)_1$ is used to determine the value of f_c. For SPICE verification, these values of the aspect ratios and corresponding values of the node capacitances are used. The typical values of the aspect ratios and the device capacitances (for $I_{Bias} = 100\ \mu$A) used for SPICE simulation are given in Table 3.3.

Table 3.3: The aspect ratios and the device capacitances for $I_{Bias} = 100\ \mu$A.

Transistors	Aspect ratio (μm/μm)	C_{DB} (pF)	C_{GDO} (pF)
M1, M2	32.0/1.0	3.2	0.25
M3, M4	18.26/1.0	1.83	0.25

3.2.9 Results and Discussion

Figure 3.7 shows the variation of f_c with the aspect ratio of the input transistors $(W/L)_1$ for different values of the bias currents I_{Bias} (10,

100, and 1000 μA). The maximum (or the optimum) value of f_c is obtained for $(W/L)_1 = 32$. This value of $(W/L)_1$ is independent of I_{Bias}. For low values of $(W/L)_1$, the values of $(W/L)_4$ are small as well. According to Eqn.(3 13), $f_c \sim \sqrt{(W/L)_1}$, as expected. For high values of $(W/L)_1$, $(W/L)_4 \approx 2(W/L)_1$ and $f_c \sim 1/\sqrt{(W/L)_1}$, i.e., the values of f_c now decreases with an increase in $(W/L)_1$. Thus, it can be inferred that the maximum value of f_c can be obtained for some intermediate value of $(W/L)_1$.

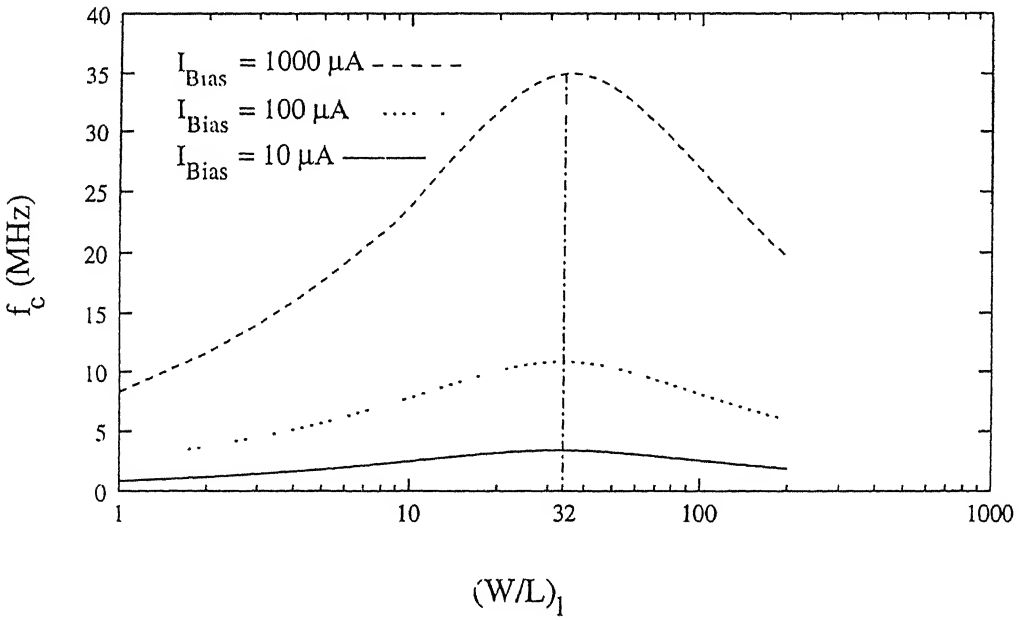


Figure 3.7: The variation of f_c with the aspect ratio of the input transistors $(W/L)_1$ predicted by the optimization routine developed in Subsection 3.2.7 for different values of I_{Bias} (10, 100, and 1000 μA).

The SPICE simulation shows reasonably good match with the results predicted from our optimization programme. Figure 3.8 shows the variation of f_c with $(W/L)_1$, obtained from SPICE simulation for different values of the bias current (10, 100, and 1000 μA). The maximum (or the

optimal) value of f_c occurs for $(W/L)_1 = 26$.

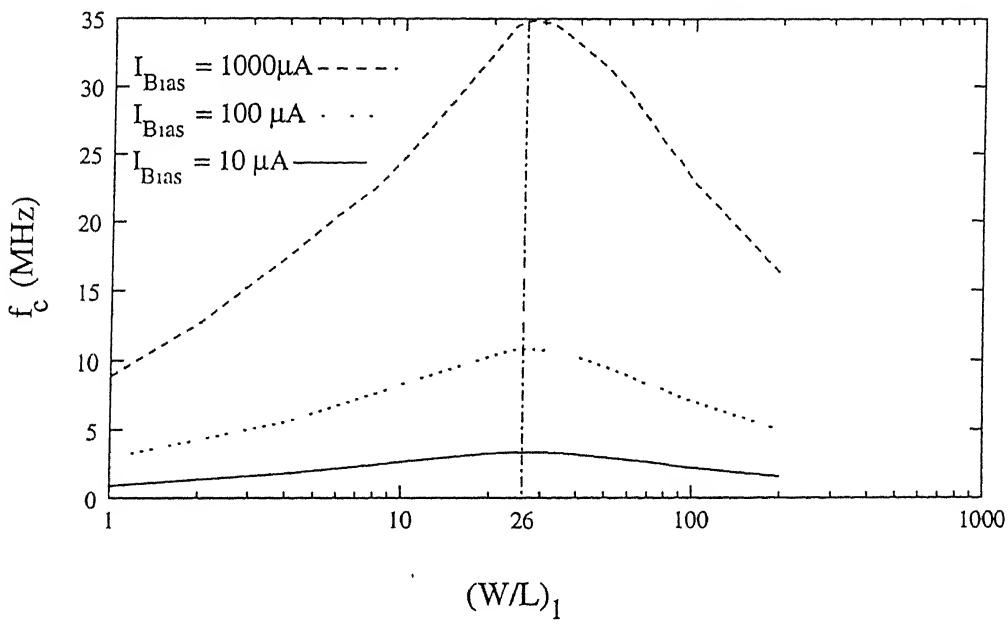


Figure 3.8: The variation of f_c with the aspect ratio of the input transistors $(W/L)_1$ for different values of I_{Bias} (10, 100, and 1000 μA), as obtained from SPICE simulation.

Figure 3.9 shows the comparison of the results obtained from the design and the SPICE simulation for $I_{Bias} = 100$ μA. There appears to be a lateral shift between the two results with the SPICE results leading the design results for f $\leq f_c$ and lagging the design results for f $\geq f_c$. The reason can be attributed to the fact that for a given value of $(W/L)_1$, Eqn.(3.14) is a cubic equation in $(W/L)_4$. Some of the roots of this cubic equation are not always of importance as these may either be negative or have very high values; and, thus, these solutions would not be physically meaningful. So, instead of finding the exact roots of this cubic equation, we have tried to extract the value of $(W/L)_4$ (in the search space $1 \leq (W/L)_4 \leq 500$), for which this cubic

Chapter 4

Design of CMOS Op-Amps for High Gain and High Unity Gain Frequency

4.1 Introduction

This chapter deals with the design aspects of CMOS op-amps for high gain and high unity gain frequency. The overall gain of the op-amp (with active load), which is a strong function of the bias point chosen for the device, can be increased by reducing the bias current. However, this change degrades the frequency response of the op-amp as we have seen in the previous chapter that the frequency response, which is also a strong function of the bias point chosen for the device, improves if the bias current is increased. It is important to note that the high unity gain frequency makes it inevitable to have a large

value of the bias current, and at the same time, in order to keep the overall gain also high, larger values of the aspect ratios of the transistors are required. Thus, the design of op-amps for high gain as well as high unity gain frequency requires more power as well as more area of the chip.

4.2 The Synthesis Procedure

In this design of the op-amp for high gain and high unity gain frequency, we have used a 2-stage CMOS op-amp configuration, as shown in Fig.4.1. The first stage is formed by the NMOS input transistors M1 and M2, the PMOS current source/active load transistors M3 and M4, and the NMOS differential-pair bias transistors M7 and M8. The second stage, which is acting as a common-source PMOS amplifier, is formed by the PMOS input transistor M6 and the NMOS load transistor M5. C_C and C_L are the compensating capacitor and the load capacitor respectively. The synthesis procedure for this configuration takes the following set of input specifications.

Performance specifications:

1. the DC open-loop gain A_{v0},
2. the unity gain frequency f_c, and
3. the load capacitance C_L.

Technological parameters:

1. the device transconductance parameters K_n' and K_p',

2. the threshold voltages V_{tn} and V_{tp}, and

3. the channel length modulation parameter λ.

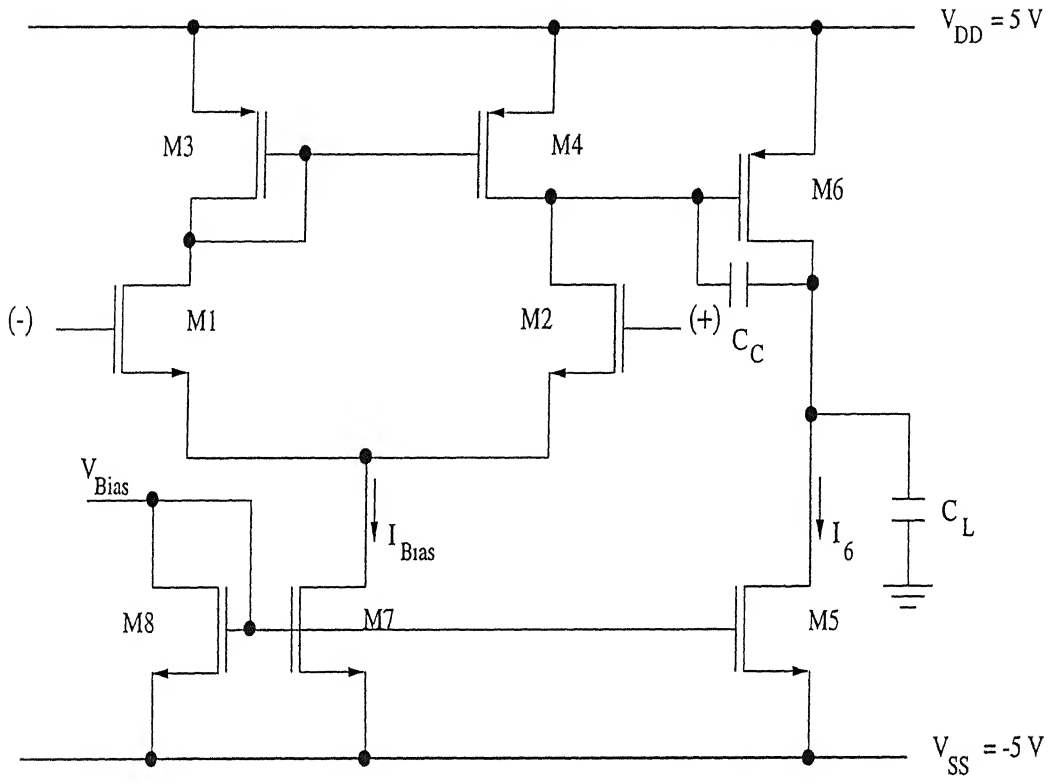


Figure 4.1: The detailed circuit diagram of the 2-stage CMOS op-amp considered in this work.

4.2.1 Mathematical Representation

The mathematical representation is based on the set of input specifications and the op-amp topology shown in Fig.4.1.

The overall gain A_{v0} is given by

$$A_{v0} = A_{v1} \times A_{v2}, \tag{4.1}$$

where A_{v1} and A_{v2} are the gains of the first stage and the second stage respectively. Substituting the standard expressions for A_{v1} and A_{v2} in the expression for A_{v0}, we get

$$A_{v0} = \frac{g_{m2}}{(g_{d2} + g_{d4})} \frac{g_{m6}}{(g_{d6} + g_{d5})}, \tag{4.2}$$

or,

$$A_{v0} \approx \frac{\sqrt{2K'_n K'_p I_{Bias} I_6 (W/L)_2 (W/L)_6}}{2\lambda^2 I_{Bias} I_6}. \tag{4.3}$$

The unity gain frequency f_c is given by

$$f_c = \frac{A_{v0}}{2\pi R_c C_C}, \tag{4.4}$$

where

$$R_c = \frac{1}{\lambda I_{Bias}} + \frac{1}{2\lambda I_6} + \frac{g_{m6}}{2\lambda^2 I_{Bias} I_6}, \tag{4.5}$$

and C_C is the compensating capacitor.

The phase margin PM is given by [12]

$$PM = 90^o - tan^{-1}(f_c/f_{nd}), \tag{4.6}$$

where

$$f_{nd} = \frac{g_{m6}}{2\pi C_L}. \tag{4.7}$$

It is clear from Eqn.(4.6) that in order to have sufficient phase margin, f_{nd} should be approximately equal to twice of f_c [12].

4.2.2 Optimization Routine

In the synthesis procedure for the op-amp considered, the optimization routine, based on the set of input specifications and the mathematical representation, has been developed in order to determine the optimal values of the design variables (i.e., I_{Bias}, I_6, and the aspect ratios of the individual transistors)[1]. The various steps of the optimization routine are as follows.

1. Using Eqn.(4.4), the value of R_c is chosen by

$$R_c = \frac{A_{v0}}{2\pi C_c f_c}. \tag{4.8}$$

2. Using Eqn.(4.7), the transconductance parameter of M6, g_{m6} is determined by

$$g_{m6} = 2\pi C_L(2f_c). \tag{4.9}$$

3. A parameter β is now defined in order to relate I_{Bias} and I_6, such that

$$\beta = \frac{I_{Bias}}{2I_6}. \tag{4.10}$$

4. Using Eqns.(4.5) and (4.10), we get a quadratic equation in I_{Bias}, given by

[1]The optimization is for either minimum power or minimum area.

$$(\lambda^2 R_c) I_{Bias}^2 = (1+\beta)\lambda I_{Bias} + g_{m6}\beta. \tag{4.11}$$

The values of I_{Bias} are obtained from this equation for different values of β.

5. I_6 is obtained using Eqn.(4.10).

6. The aspect ratio of the transistor M6, $(W/L)_6$ is determined by

$$(W/L)_6 = \frac{g_{m6}^2}{2K_p' I_6}. \tag{4.12}$$

7. The gain of the second stage A_{v2} is determined by

$$A_{v2} = \frac{g_{m6}}{2\lambda I_6}. \tag{4.13}$$

8. Using Eqn (4.1), the gain of the first stage A_{v1} is determined by

$$A_{v1} = \frac{A_{v0}}{A_{v2}}. \tag{4.14}$$

9. The transconductance parameter of the input transistors g_{m2} is obtained by

$$g_{m2} = \frac{A_{v1}}{\lambda I_{Bias}}. \tag{4.15}$$

10. The aspect ratio of M2, $(W/L)_2$ is determined by

$$(W/L)_2 = \frac{g_{m2}^2}{K_n' I_{Bias}}. \tag{4.16}$$

11. For a chosen value of the aspect ratio $(W/L)_7$ $(= (W/L)_8)$ of the transistors used in the differential-pair bias subblock, the value of V_{Bias} is given by the Eqn.(2.21).

12. For a chosen value of $(W/L)_7$, the aspect ratio of M5, $(W/L)_5$ is determined by

$$(W/L)_5 = (W/L)_7/2\beta. \tag{4.17}$$

4.2.3 Implementation

Based on the optimization routine, a programme is written in the C-language in order to predict the optimal values of the design variables, i.e, I_{Bias}, I_6, and the aspect ratios of the individual transistors. It also predicts the variations in the sum of the currents flowing through the two stages (i.e., $I_{Bias} + I_6$), and the total area of the op-amp as a function of β. The input specifications for A_{v0} and f_c used in this design of the op-amp are 90 dB and 10 MHz respectively. The following parameters have been used for optimization.

K_n'	:	82 $\mu A/V^2$	K_p'	:	41 $\mu A/V^2$
V_{tn}	:	0.7 V	V_{tp}	:	-0.8 V
C_L	:	10 pF	C_C	:	10 pF
C_{BD}	:	0.75 pF	C_{GDO}	:	0.15 pF
C_{GSO}	:	0.1 pF	λ	:	0.01 V^{-1}

From the optimizer, a typical set of the values of the design variables for minimum power ($\approx$ 7.09 mW) are obtained, which are shown in Table 4.1

and used for the SPICE simulation for cross-verification of the design.

Table 4.1: A typical set of the values of the design variables obtained from our optimizer for minimum power ($\approx$ 7.09 mW) and are used for the SPICE simulation.

Transistor	W/L (μm/μm)	Current through transistor (μA)
M1, M2	13.80/1.00	177.41
M3, M4	27.14/1.00	177 41
M6	54.27/1.00	354.82
M5	20.00/1.00	354.82
M7, M8	20.0/1.0	354.82

4.2.4 Results and Discussion

Figures 4.2 and 4.3 show the variations of the total current ($I_{Bias} + I_6$) and the total area of the op-amp respectively as a function of β. These are obtained for the given input specifications of A_{v0} and f_c. It is clear from these figures that the value of β for which the total current is minimum is different from the value of β for which the total area of the op-amp is minimum. This is an example which shows the conflicting nature of the constraints, more specifically, the power consumption and the total area of a circuit never go hand-in-hand, i.e., both can not be minimized simultaneously.

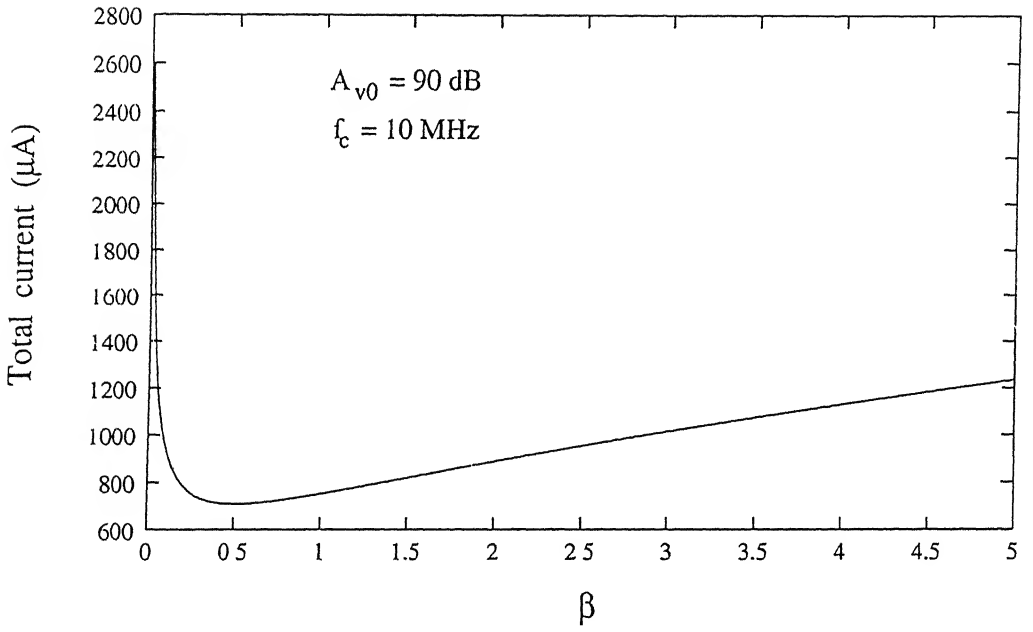


Figure 4.2: The variation of the total current (i.e., $I_{Bias} + I_6$) as a function of β with $A_{v0} = 90$ dB and $f_c = 10$ MHz.

The SPICE simulation of our design shows reasonably good match with our design results over the entire range of β. Table 4.2 shows the comparison of the results obtained from our design and the SPICE simulation for a particular set of performance specifications.

Table 4.2: The comparison of the results obtained from our design and the SPICE simulation.

Specs	Design	SPICE
A_{v0} (dB)	90	90.04
f_c (MHz)	10	10.0

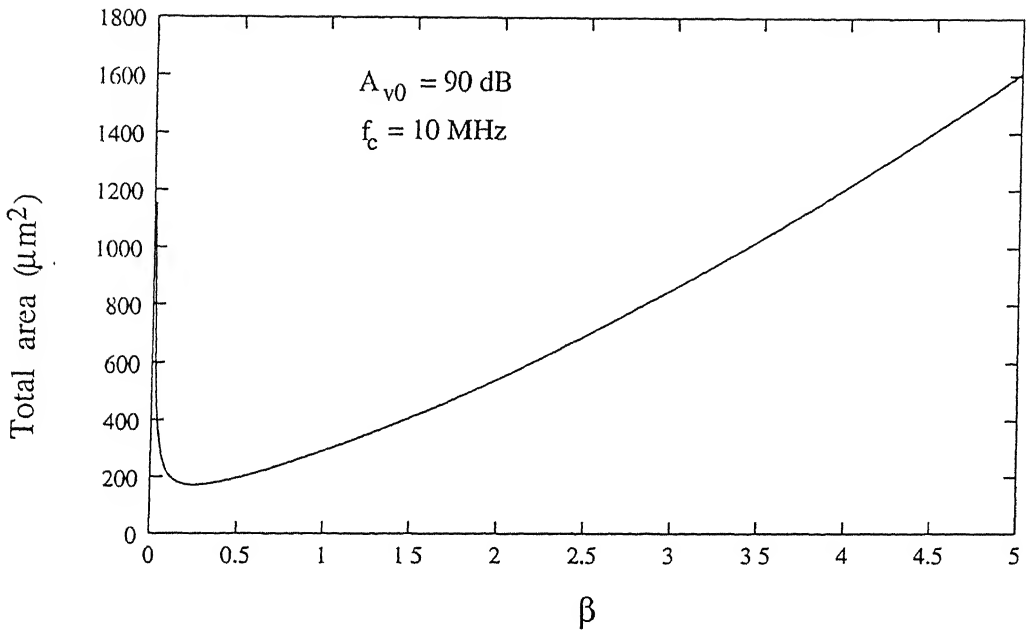


Figure 4.3: The variation of the total area as a function of β with $A_{v0} = 90$ dB and $f_c = 10$ MHz.

Figures 4.4 and 4.5 show the gain plot and the phase plot respectively, highlighting the phase margin obtained from the design. The two plots have been obtained for the design variables corresponding to the minimum power (≈ 7.09 mW). Although the system has a phase margin of 39°, it is not stable because the circuit displays a right half-plane zero along with two poles. Physically, the zero arises because the compensating capacitor provides a path for the signal to propagate directly through the circuit to the output at high frequencies. Since there is no inversion in that signal path as there is in the inverting path dominant at low frequencies, stability is degraded. For low frequencies, the circuit behaves like an integrator, but at high frequencies, the compensating capacitor behaves like a short circuit. When this occurs, the second stage behaves like a diode-connected transistor, presenting a load to the first stage, which is equal to $1/g_{m6}$. Thus, the circuit displays a gain at

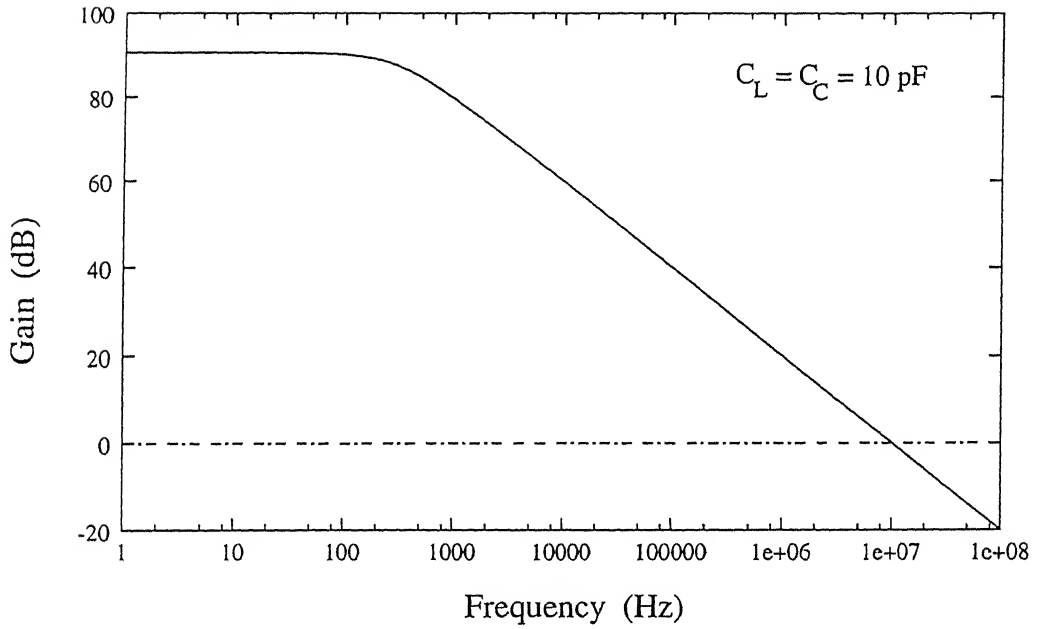


Figure 4.4: The gain versus frequency plot of the 2-stage CMOS op-amp obtained using the optimized values of the aspect ratios of the transistors under the constraint of minimum power (≈ 7.09 mW).

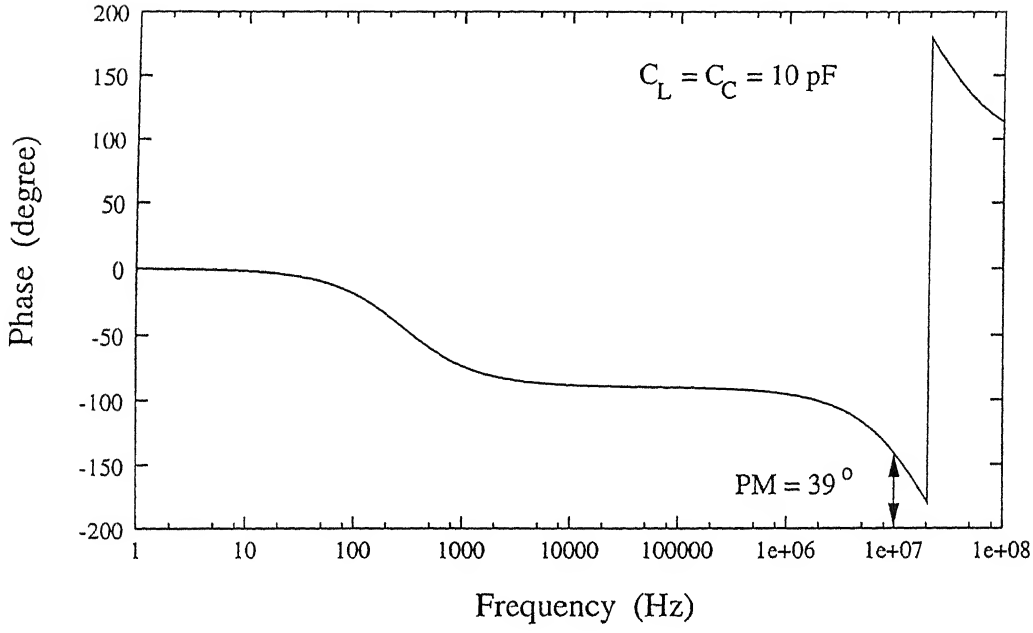


Figure 4.5: The phase versus frequency plot of the 2-stage CMOS op-amp obtained using the optimized values of the aspect ratios of the transistors under the constraint of minimum power ($\approx$ 7.09 mW).

high frequencies which is simply equal to g_{m1}/g_{m6}. The polarity of this gain is opposite to that at low frequencies, turning any negative feedback that might be present around the amplifier into a positive feedback.

A simple approach for eliminating the effect of the right half-plane zero is to insert a nulling resistor R_z ($\geq 1/g_{m6}$) in series with the compensating capacitor (as verified by SPICE). Figure 4.6 shows the phase plot with the nulling resistor $R_Z \approx 796\ \Omega$. This value is determined by the relationship $R_Z = 1/g_{m6}$, where g_{m6} is given by Eqn.(4.9).

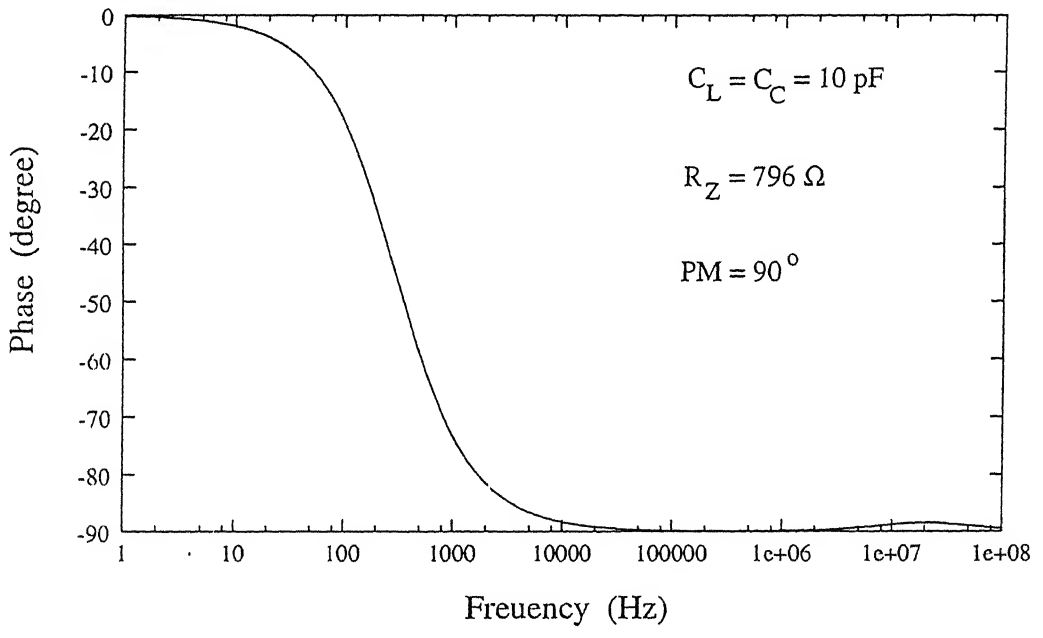


Figure 4.6: The phase versus frequency plot of the 2-stage CMOS op-amp obtained using the optimized values of the aspect ratios of the transistors under the constraint of minimum power ($\approx$ 7.09 mW) with the nulling resistor $R_Z \approx 796\ \Omega$.

There is an inherent limitation of the synthesis procedure devel-

oped in this chapter. The design variables for high input values of f_c (even of the order of 50 MHz) are physically not possible because values of the design variables will be unrealistically high (e g., I_{Bias} will be of the order of 2-10 mA, and the aspect ratios will be of the order of 100 or more). The reason for this lies in the mathematical representation, and, hence, in the optimization routine developed in this chapter. We have used the well known square-law characteristic of the MOS transistor (i.e., $I = (K'_n/2)(W/L)(V_{GS} - V_{tn})^2$) for the design of the op-amp for high gain and high unity gain frequency. Using this relationship, it is not possible to have very high gain (of the order of 90 dB) as well as high unity gain frequency (of the order of 50 MHz or more) simultaneously. A very high value of f_c can be obtained, if very short channel devices (with L $\leq 1\mu m$) in combination with large gate-source voltages are used, where the degradation effects of high electric fields in the MOS transistors have to be incorporated. Thus, the well known square-law characteristic needs to be properly modified accordingly.

We have developed a design for a 2-stage CMOS op-amp based on short channel devices, but the cross verification of this design using SPICE was not possible as the effect of degradation of the high electric fields is not properly supported by the SPICE package available to us.

In the next chapter, the design and optimization procedure for CMOS op-amps under the constraint of high slew rate is presented.

Chapter 5

Design of CMOS Op-Amps for High Slew Rate

5.1 Introduction

This chapter deals with the design aspects of CMOS op-amps for high slew rate. Slewing, which is a non-linear (large-signal) phenomenon, limits the rate at which the output voltage can change with respect to time (i.e., dV_o/dt). This limitation results because of the limited current sourcing/sinking capability of the circuit in order to charge/discharge the compensating and/or load capacitor(s). In this design of the op-amp for high slew rate, we have used a 2-stage CMOS op-amp configuration, as shown in Fig.4.1. Prior to the arrival of the input step at the gate of M1, the currents in M1 and M2 are both equal to $I_{Bias}/2$. After the large step occurs at the input of M1, it conducts more current and cuts off M2. Hence, the current conducted by both

M1 and M3 are now equal to I_{Bias}. Since M3 and M4 form a current mirror, the current in M4 (which charges C_C) is also equal to I_{Bias}. Hence, assuming the second stage can sink the current I_{Bias}, the slew rate (SR) is given by

$$SR = \frac{dV_o}{dt} = \frac{I_{Bias}}{C_C}. \tag{5.1}$$

Equation (5.1) shows that the slew rate is a linear function of the bias current with the slope equal to $1/C_C$. Thus, it can be increased by

1. simply increasing the bias current, at the cost of higher power,

or

2. choosing the bias current and the value of C_C in a combination provided that the stability of the system is maintained.

The second option has been utilised in this design of CMOS op-amps. It is clear that this would give higher value of the slew rate with less power consumption than the first option.

5.2 The Synthesis Procedure

The mathematical representation described in Chapter 4 has been used for the design of the op-amp for high slew rate and the synthesis procedure takes the same set of input specifications which has been described in Chapter 4.

5.2.1 Optimization Routine for the Design of the 2-stage CMOS Op-Amp

In the synthesis procedure for the op-amp considered, the optimization routine, based on the set of input specifications and the mathematical representation, has been developed in order to maximize the slew rate of the op-amp. The various steps are as follows.

1. The value of the compensating capacitor C_C is determined by

$$C_C = \frac{C_L}{n}, \tag{5.2}$$

   where n is a real number.

2. R_c is determined by Eqn.(4.8) for different values of n.

3. The transconductance parameter of M6, g_{m6} is determined by Eqn.(4.9).

4. For 10 μA $\leq I_6 \leq$ 500 μA, the aspect ratio of M6, $(W/L)_6$ is obtained by Eqn.(4.12).

5. The gain of the second stage A_{v2} is determined by Eqn.(4.13).

6. The gain of the first stage A_{v1} is determined by Eqn.(4.14).

7. Using Eqn.(4.5), the value of I_{Bias} is determined by

$$I_{Bias} = \frac{(2\lambda I_6 + g_{m6})}{\lambda(2\lambda R_c I_6 - 1)}. \tag{5.3}$$

8. The transconductance parameter of the input transistors g_{m2} is obtained by Eqn.(4.15).

9. The aspect ratio of M2, $(W/L)_2$ is determined by Eqn.(4.16).

10. The slew rate SR is given by Eqn.(5.1)

11. For a chosen value of the aspect ratio$(W/L)_7$ $(= (W/L)_8)$ of the transistors used in the differential-pair bias subblock, the value of V_{Bias} is given by Eqn.(2.21).

12. The aspect ratio of M5, $(W/L)_5$ is determined by

$$(W/L)_5 = \frac{(W/L)_7 I_6}{I_{Bias}}. \tag{5.4}$$

5.2.2 Implementation

Based on the optimization routine, a programme is written in the C-language in order to predict the variation of the slew rate (SR) of the op-amp as a function of I_{Bias} for two different chosen values of C_C (8 and 10 pF). It also predicts the design variables, i.e., I_{Bias}, I_6, and the aspect ratios of the individual transistors. These values of the design variables are fed to a SPICE file for cross-verification of the design. The input specifications for A_{v0} and f_c used in this design of the op-amp are 80 dB and 2 MHz respectively. The parameters used in chapter 4 have been used in this design of the op-amp for high slew rate.

From the optimizer, a typical set of the values of the design variables for a chosen value of C_C (= 10 pF) are obtained. These values are used for the SPICE simulation and are shown in Table 5.1.

Table 5.1: A typical set of the values of the design variables for a chosen value of C_C (= 10 pF) used for SPICE simulation.

Transistor	W/L (μm/μm)	Current through transistor (μA)
M1, M2	1.00/1.00	98.87
M3, M4	11.61/1.00	98.87
M5	8.19/1.00	81.00
M6	9.51/1.00	81.00
M7, M8	20.00/1.00	197.74

5.2.3 Results and Discussion

Figure 5.1 shows the variation of the slew rate (SR) of the op-amp as a function of I_{Bias} for two different chosen values of C_C (8 and 10 pF). This is obtained for the given input specifications for A_{v0} and f_c. It is clear from the figure that the same value of the slew rate can be obtained for lesser value of I_{Bias} corresponding to C_C = 8 pF as compared to the corresponding value for C_C = 10 pF.

The SPICE simulation of our design shows reasonably good match with the results obtained from our optimizer, which has been verified over the entire range of the design variables Table 5.2 shows the comparison of the results obtained from our design and the SPICE simulation for a particular set of performance specifications.

Figures 5.2 and 5.3 show the gain plot and the phase plot respectively, highlighting the phase margin obtained from the design. The two

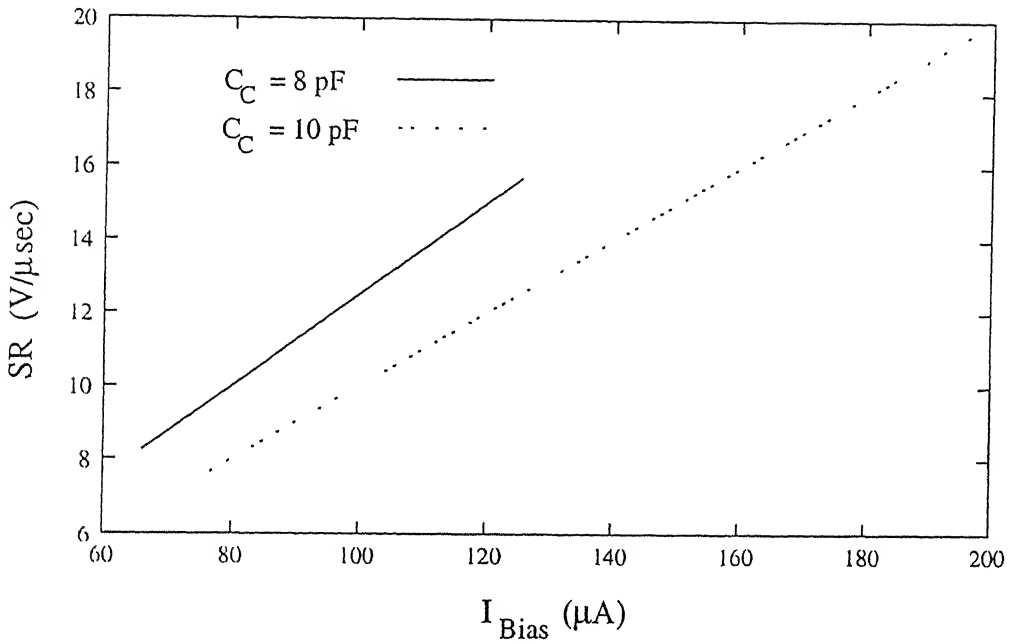


Figure 5.1: The variation of the slew rate of the op-amp as a function of I_{Bias} for different chosen values of C_C (8 and 10 pF) with $A_{v0} = 80$ dB and $f_c = 2$ MHz.

plots have been obtained for the design variables listed in Table 5.1 with nulling resistor $R_Z \approx 4$ kΩ in series with the compensating capacitor C_C in order to avoid the instability in the system caused by the right half-plane zero.

Table 5.2: The comparison of the results obtained from our design and the SPICE simulation.

Specs.	Design	SPICE
A_{v0} (dB)	80	81.04
f_c (MHz)	2	2.04
SR (V/μsec)	19.77	19.49

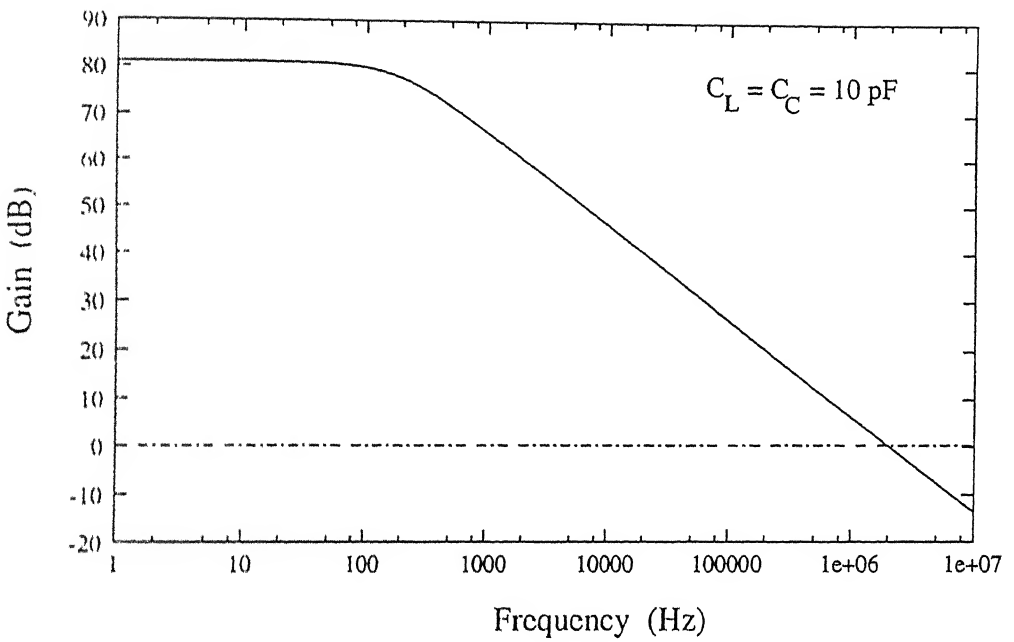


Figure 5.2: The gain versus frequency plot of the 2-stage CMOS op-amp obtained using the design variables listed in Table 5.1 with nulling resistor $R_Z \approx 4$ kΩ.

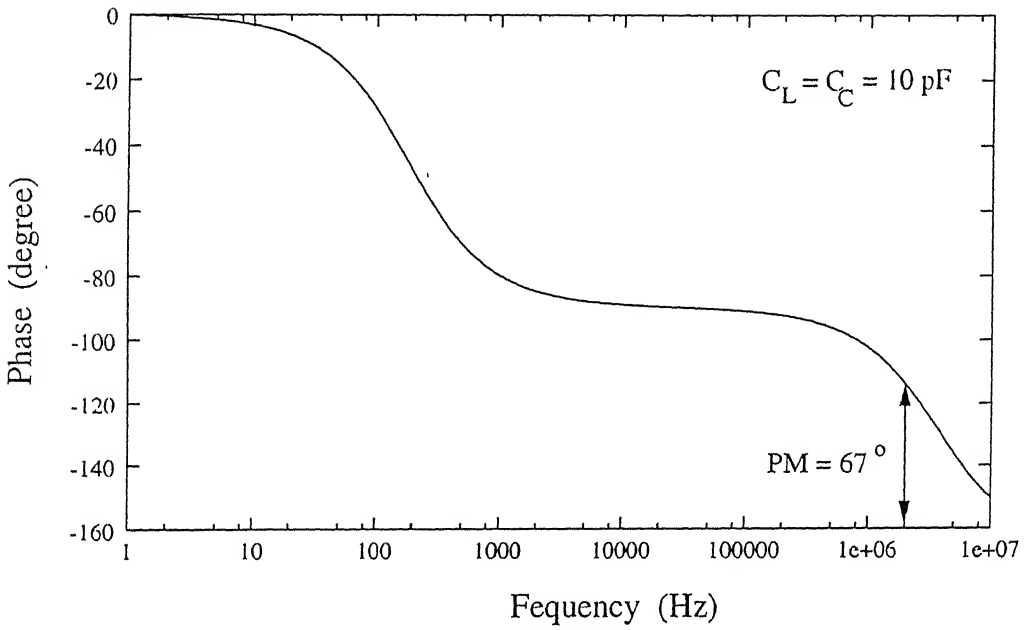


Figure 5.3: The phase versus frequency plot of the 2-stage CMOS op-amp obtained using the design variables listed in Table 5.1 with nulling resistor $R_Z \approx 4$ kΩ.

Thus, the synthesis procedure developed in this chapter for the design of the 2-stage CMOS op-amp for high slew rate, can be used to obtained the maximum value of the slew rate (SR) for a given set of input performance specifications (in our case, these are A_{v0} and f_c). Different combinations of these input performance specifications would give rise to different ranges of the slew rate, and, hence, its maximum obtainable values; however, for a given set of input specifications, the maximum obtainable value of the slew rate is a fixed quantity. It is important to note that the set of input performance specifications in some sense acts like a constraint, i.e., the slew rate is maximised for the given values of A_{v0} and f_c.

Chapter 6

Summary and Conclusion

In this work, we have tried to present the state of analog design automation and its associated problems. The design methodologies and the synthesis algorithms for the design of CMOS op-amps under several constraints are given, which may be extended to other analog blocks. We have developed the synthesis procedure (including the optimization routine) for CMOS op-amps for a wide variety of specifications appropriate for complex analog systems (e.g., minimum power and area, high bandwidth, high gain and unity gain frequency, and high slew rate). Synthesis procedure for each such design starts with a set of input specifications. The optimization routine developed provides the design variables (i.e., the lengths and widths of individual transistors, the bias currents, the compensating capacitor values, etc.), which are fed to a SPICE file for the cross-verification of the design.

In the design of CMOS op-amps for minimum power and area, we started with the synthesis procedure for a simple current mirror, as given by OASYS. The alarmingly high percent error between the results obtained from

the design and the SPICE simulation led us to develop our own optimization routine, which provided far better results than those predicted by OASYS. A model for the channel length modulation parameter has also been developed in this work. Synthesis procedure for a symmetric CMOS op-amp is also given and the results have been verified using SPICE simulation.

In the design of CMOS op-amps for high bandwidth, we started of with the synthesis procedure developed without taking into account the effect of the sizes of the individual transistors on the node capacitances. It was inferred that any value of the unity gain frequency f_c was obtainable at the higher cost of either power or area or both, however, the improved synthesis procedure developed in this work, which included the device capacitances suggested that f_c can not be increased indefinitely at the higher cost of area - a fact verified in this work.

Two modifications in the design of the op-amp for high bandwidth are possible.

1. If the slew rate (SR) is one of the input specifications for the design of the op-amp for high bandwidth, then the minimization of the power consumed by the op-amp leaves us with the choice of choosing the minimum value of the bias current (using SR $\leq I_{Bias}/C_L$), and, consequently, a high value of f_c can only be obtained with a correspondingly higher total area of the op-amp. This is one way we can go for both power and area optimization.

2. With the same input specifications as given in Subsection 3.2.1, both power and area minimization is also possible, but in a different way. From Eqn.(3.11), it is clear that for a given value of f_c, the bias current

I_{Bias} and the aspect ratio of the input transistors $(W/L)_1$ can be related by

$$I_{Bias} = \frac{2\pi^2 f_c^2 (C_{n5} + C_L)^2}{K_n'} \frac{1}{(W/L)_1}. \tag{6.1}$$

Using Eqns.(3.10) and (6.1), a programme is written in the C-language in order to predict the variation of I_{Bias} with the total area of the op-amp for $f_c = 10$ MHz, which is shown in Fig.6.1. This is another way we can go for both power and area minimization.

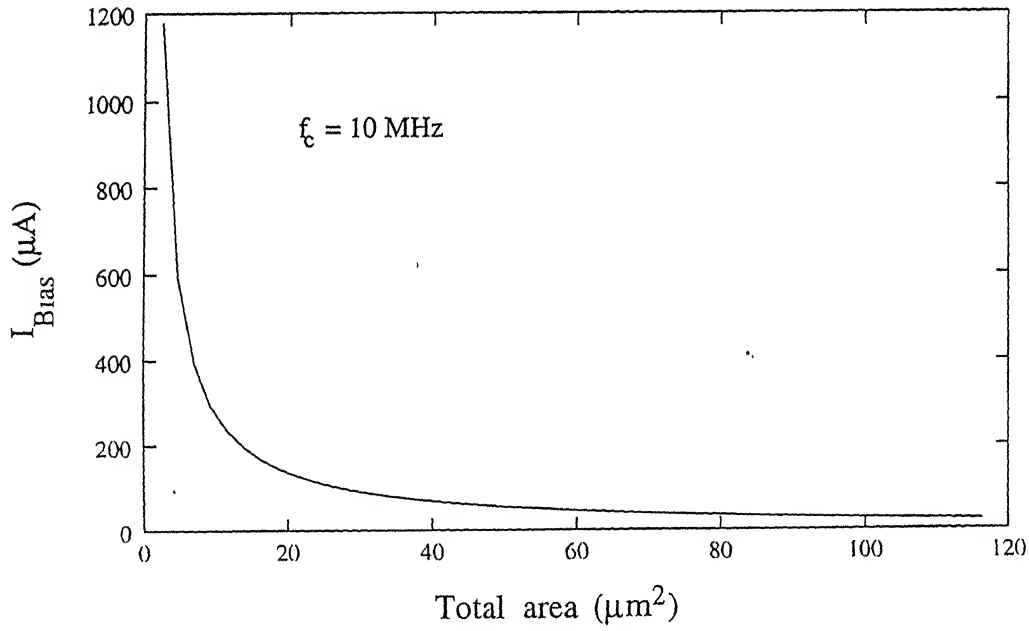


Figure 6.1: The variation of I_{Bias} with the area of the op-amp for $f_c = 10$ MHz.

In the design of CMOS op-amps for high gain and high unity gain frequency, a nulling resistor in series with the compensating capacitor has been used in order to avoid the instability caused by a right half-plane zero.

The synthesis procedure developed for this design has its own limitations for very high input specification of f_c (of the order of 50 MHz or more). This is because of the mathematical representation used in this design. We have used the well known square-law characteristics of the MOS transistor ($I = (K'_n/2)(W/L)(V_{GS}-V_{tn})^2$). In order to get the unity gain frequency of the order of 50 MHz or more, the short channel devices in combination with large gate-to-source voltages have to be used. The well known square-law characteristics have to be modified in order to incorporate the degradation effects of high electric fields. Our attempt to design the op-amp using short channel devices could not be substantiated because the SPICE package available to us does not support the degradation effects of high electric fields properly.

In the design of CMOS op-amps for high slew rate, we have chosen the values of the bias current and the compensating capacitor in a combination in order to get a high value of the slew rate, provided the stability of the system is maintained. This is the basis of the optimization routine developed.

In the process of developing the synthesis procedure, we have realised that another synthesis approach for the design of the 2-stage CMOS op-amp for high slew rate can be adopted, which would be based on the set of input specifications with the midband gain A_{v0} and the load capacitance C_L as its elements. In this particular synthesis procedure, the unity gain frequency would not be fixed. The implementation and the SPICE verification of the design based on this idea is being left as a future task.

All the results obtained from the designs of the op-amps considered in this work showed excellent match with the results obtained from

SPICE simulations. The percent error between the results obtained from our design and the SPICE simulations is less than 6% for all the designs considered in this work

It has been realised in this work that the development of the synthesis procedure for op-amps (and, in general, for analog circuits) depends strongly on the set of input specifications, constraints, and the circuit topology used. Thus, the synthesis procedure for the op-amps (and, in general, analog circuits) based on the design methodology and synthesis algorithm presented in this work would vary for different sets of specifications, constraints, and the circuit topology. Thus, development of analog cell libraries based on the design methodology and synthesis algorithm will prove to be a time consuming job as the inclusion of a new circuit would require the development of a new synthesis procedure (including the optimization routine) for it. Our design methodology and synthesis procedure, like other analog circuit synthesis tools, require an intensive knowledge of analog circuits.

The following conclusions can be drawn from the design aspects of CMOS op-amps for various specifications considered in this work.

- The synthesis procedure presented in this work would prove to be helpful in its development for op-amps for other specifications and its verification using SPICE, which have not been considered in this work.

- The actual development of the synthesis procedure would greatly depend on the designer's experience, and the total time taken in its development and subsequent verification by SPICE would vary from designer-to-designer.

- The performance specifications in some sense act like constraints.

• The number of the set of design variables in the search space are strongly dependent on the individual values of the elements of the set of input specifications.

We had started the work with the view to develop a design, synthesis, and optimization tool for CMOS op-amps for various specifications. We have developed the synthesis procedures for 1/2-stage CMOS op-amp for various specifications, but certain issues still have to be considered. A solid foundation has been led for the development of an analog design, synthesis, and optimization tool for op-amps. The following steps have to be taken before writing the code for the tool.

• Design and optimization of CMOS op-amps based on the possible changes or improvements discussed in this chapter.

• Determination of the range of performance specifications, given as inputs to the optimization routine, for each design considered in this work.

• Development of the synthesis procedure and its verification by SPICE for 2-stage CMOS op-amps for high PSRR (power supply rejection ratio), high CMRR (common mode rejection ratio), and low output resistance.

• Development of the synthesis procedure for 3/4-stage CMOS op-amps for various specifications.

References

1. M. G. R. Degrauwe, O. Nys and H. J. Oguey, "IDAC: an Interactive Design Tool for Analog CMOS Circuits", IEEE J. of Solid-State Circ., vol.SC-22, no.6, pp.1106-1115, 1987.

2. R. Harjani, R. A. Rutenbar and L. R. Carley, "OASYS: a Framework for Analog Circuit Synthesis", IEEE Trans. on CAD, vol.8, no.12, pp.1247-1266, 1989.

3. H.Y. Koh, C. H. Sequin and P. R. Gray, "OPASYN: a Compiler for CMOS Operational Amplifiers", IEEE Trans. on CAD, vol.9, no.2, pp.113-125, 1990.

4. J. H. Huijsing and W. Sansen, "Analog Circuit Design", Kluwer Academic Pubishers, London, 1993.

5. D.M.W. Leenaerts, "TOPICS, a Contribution to Analog Design Automation", Ph.D. Thesis, University of Technology Eindhoven, 1992.

6. Silicon and Software Systems, MIDAS: A knowledge based Analog Synthesis Environment, User's Guide.

7. H. Yanghutiel, A. Sangiovanni-Vincentelli and P. R. Gray, "Methodology for

Automated Layout Switched -Capacitor Filters", Proc. IEEE ICCAD, pp.444-447, 1986.

8. G. Jusuf, P. R. Gray, A. Sangiovanni-Vincentelli and P. R. Gray, "CADICS - Cylic Analog-to-Digital Converter Synthesis", Proc. IEEE ICCAD, pp 286-289, 1990.

9. Rajeev Ranjan and Vishal Gupta, "Approaches to Design Automation - a case study", B. Tech. Project Report, IIT Kanpur, 1998.

10. M. H. Rashid, SPICE for Circuits and Electronics using PSPICE, Prentice Hall of India, New Delhi, 2nd Edition, 1996.

11. P. R. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley and Sons, New York, 3rd Edition, 1993.

12. K. R. Laker and W. M. C. Sansen, "Design of Analog Integrated Circuits and Systems", McGraw-Hill, Hightstown, 1994.